2017 IEEE Electrical Design of Advanced Packaging & Systems Symposium

EDAPS 2017

Haining, Hangzhou, Dec. 14-16

TECHNICAL PROGRAM

IEEE

IEEE ELECTRONICS PACKAGING SOCIETY

Dec.13 Wednesday	**14:00-17:30**	**Registration**	**Yuanzheng Hotel, Haizhou Hotel**	
	7:30-9:00	Registration	1st Floor, Multimedia Hall	
	9:00-9:15	Opening Ceremony	Address from EDAPS Co-Chair：Er-Ping Li	
	9:15-12:00 Keynote Presentations	9:15-10:00	Stochastic Electromagnetic Field Modeling for EMI/EMC-Aware Design of Electronic Systems	Andreas C Cangellaris
		10:00-10:30	Coffee Break	
		10:30-11:15	2D Materials for Smart Life	Kaustav Banerjee
		11:15-12:00	Integrating thermal, electrical, and materials issues for extreme-density power electronics	Philip T. Krein
	12:00-13:30	**Lunch**		
Dec.14 Thursday	**Rooms**	**201, Lecture Theatre West**	**204, Lecture Theatre West**	**207, Lecture Theatre West**
	13:30-14:00	Tut1	Tut2-1	Wor4-1
	14:00-14:30		Tut2-2	Wor4-2
	14:30-15:00	Wor3-1	Tut2-3	Wor1-1
	15:00-15:30	Wor3-2	Tut2-4	Wor1-2
	15:30-15:50	**Coffee Break**		
	15:50-16:20	Wor3-3	Tut3-1	Wor1-3
	16:20-16:50	Wor2-1	Tut3-2	Wor1-4
	16:50-17:20	Wor2-2	Tut3-3	Wor1-5
	17:20-17:50	Wor2-3	Tut3-4	Wor1-6
	17:50-18:20	Wor2-4	Tut3-5	Wor1-7
	18:30-21:00	**Reception**		
Dec.15 Friday	Keynote Presentations	8:00-8:45	3D-IC Technology: Reliability Challenges and Biomedical Application	Tetsu Tanaka
		8:45-9:30	Signal Integrity Designs of HBM in 3D Packaging	Jun Fan
	9:30-9:50	**Coffee Break**		
	Rooms	**201, LTW**	**204, LTW**	**207, LTW**
	9:50-12:10	Oral Session 1	Oral Session 2	Oral Session 3
	12:10-13:30	**Lunch**		
	13:30-15:30	Poster：Multimedia Hall		
		Oral Session 4-1		Oral Session 6-1
	15:30-15:50	**Coffee Break**		
	15:50-17:50	Oral Session 4-2	Oral Session 5	Oral Session 6-2
	19:00-21:30	**Gala Dinner/Best Paper Award Presentation**		
Dec.16 Saturday	**Rooms**	**201, LTW**	**204, LTW**	**207, LTW**
	8:00-10:00	Oral Session 7-1	Oral Session 8-1	Oral Session 9-1
	10:00-10:20	**Coffee Break**		
	10:20-12:20	Oral Session 7-2	Oral Session 8-2	Oral Session 9-2
	12:20-13:30	**Lunch**		
	13:30-15:30	Oral Session 10-1	Oral Session 11-1	Oral Session 12-1
	15:30-15:50	**Coffee Break**		
	15:50-17:50	Oral Session 10-2	Oral Session11-2	Oral Session 12-2

EDAPS 2017

2017 IEEE Electrical Design of Advanced Packaging & Systems Symposium

Final Technical Program

December 14-16, 2017
Haining, Hangzhou, China

www.edaps2017.org

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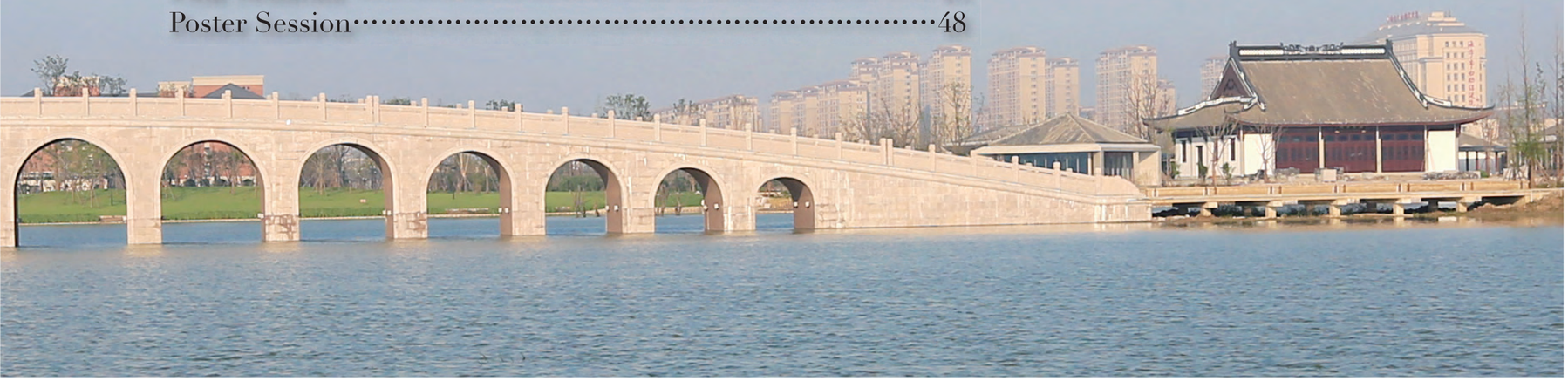


Greetings from 2017 EDAPS General Co-Chairs

It is our great pleasure to invite you to attend the 2017 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium. EDAPS has been one of the main events in the Asia Pacific region with a focus on the electrical design of chips, packages and systems for electronics applications. For more than a decade, this symposium has attracted world class researchers from both academia and industry to share their state-of-the-art results in chips, packages and printed circuit board designs and measurements. The symposium consists of keynotes and invited talks from experts, paper presentations, industry exhibition, tutorials and an informal social setting for networking.

EDAPS is sponsored by the IEEE Components, Packaging and Manufacturing Technology Society. The EDAPS 2017 will be held in Haining, Hangzhou, China. EDAPS is an excellent forum to highlight the latest advances in the high-speed and high-performance semiconductor industry. Engineers and researchers will engage in the 3 full day conference and workshop, to be held during December 14-16 in Haining. The forum offers a great opportunity for sponsorships and for the related companies to build their brands in this leading international platform.

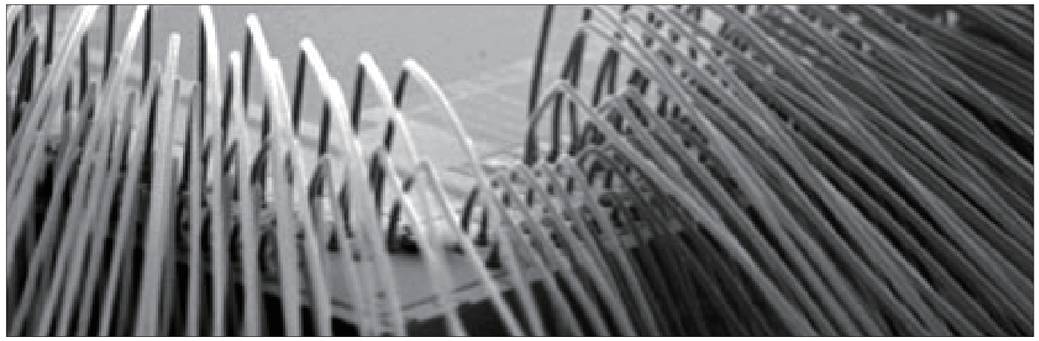
Hangzhou is the capital and most populous city of Zhejiang Province in east China. It is one of the most important sightseeing cities in china with its many historic places and beautiful scenery. We hope all of attendees an enjoyable and memorable stay in Hangzhou, China.

Prof. Wen-Yan Yin and Prof. Erping Li,

General Co- Chairs

Prof. Wen-Yan Yin

Prof. Er-Ping Li



Message from the Technical Program Co-Chairs

On behalf of the Technical Program Committee (TPC), we welcome all of you to attend the 2017 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium in Hangzhou, one of the most ancient cities in China.

Along with 65 members, EDAPS 2017 TPC has worked together and generated a diverse and well-organized technical program, which covers nearly all topics that are important to the advanced packaging and systems. Keeping the traditionally high standards of EDAPS, the technical program has broken several records set by earlier conferences. A high number of 187 papers were submitted to EDAPS, where 144 papers were from mainland China and 43 papers were from overseas distributed in 10 countries and regions. More than 60 TPC members reviewed the papers for their technical merits and interests to the advanced packaging and systems. Finally a total number of 166 papers were accepted, including 30 invited papers, for presentation in EDAPS 2017. We have arranged 136 oral sessions from Friday to Saturday to present the papers.

Workshops will be held on Thursday, before the regular EDAPS 2017 presentations. There are 4 workshops contributed by the academy and industry in this year on, PEEC Modeling for Signal Integrity and EMC Analysis, Multiphysis Modeling and Simulation for Advanced Integration and Packaging, Analyzing Power Supply Induced Jitter in I/O Buffers: from Simple to Complex and Machine Learning for Hardware Design. Three tutorials are also contributed by the academy and industry, High-Speed Circuit Modeling and Design Using X Parameters, Achieving Power Integrity through a Systematic Physics-Based and Interconnect Characterization and IPC D24D Standard.

This year all paper submissions, paper review and evaluation, and paper acceptance process are on-line based. We are indeed proud of the excellent work done by all the local co-organizers and session organizers. We would like to thank them very much for their great efforts on the technical supports.

Prof. Junfa Mao, and Prof. Gaofeng Wang

Technical program Co-Chairs

Prof. Junfa Mao

Prof. Gaofeng Wang

Technical Program Committee Vice Co-Chairs

Prof. Kai Kang

Prof. Liang Zhou

Prof. Dazhi Ding

Prof. Yang Xu

Prof. Linsheng Wu

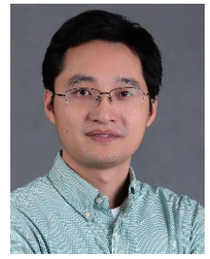
Local Organization Committee Co-Chairs

Prof. Liandong Wang

Prof. Xueqin Yi

Prof. Yinshui Xia

Prof. Zhixiang Huang



Prof. Qingfeng Zhang

Local Co-Organizers

Sponsors

EDAPS 2017 Committee Officers

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Wen-Yan Yin, Erping Li
Technical Program Committee Co-Chairs
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Technical Program Committee Vice Co-Chairs
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Local Organization Committee Co-Chairs
Liandong Wang, Xueqin Yi, Qingfeng Zhang, Zhixiang Huang, Yingshui Xia
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Yang Du, Xiaopeng Yu
Conference Secretary
Cheng Ning, Xinran Zhu (Sharon)

EDAPS 2017 TPC Members

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Andreas Cangellaris	Ran Hao	Christan Schuster	Yongle Wu
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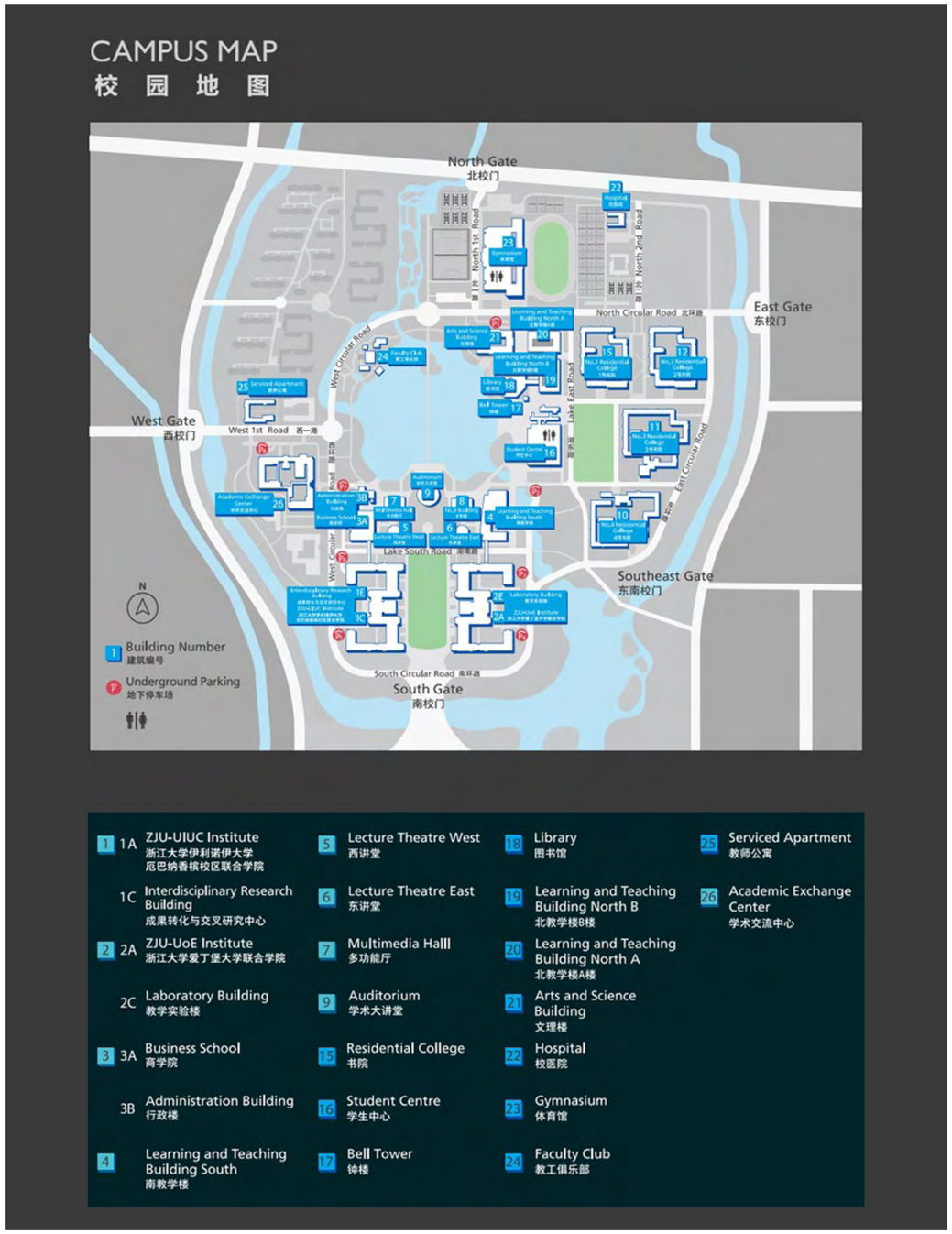
Zhenhong Fan	Taijun Liu	Jian Wang	Xiuying Zhang
Ling Feng	Kaixue Ma	Liandong Wang	Yue Ping Zhang
Pingqi Gao	Antonio Maffucci	Yali Wang	Wensheng Zhao
Dries Vande Ginste	Ivan Ndip	Xingchang Wei	Yi Zhao
			Cheng Zhuo

Conference Site and Office Location

2017 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium will be held on 14th -16th Dec. at Multimedia Hall of the international campus, Zhejiang University, in Haining Hangzhou, CHINA. The office and Section locations are shown in campus map.



Registration

The EDADS 2017 Registration begins on 14th, Dec. 2015. The registration desk is Multimedia Hall of the international campus. The on-site registration fee is shown in the table.
The on-site student registration requires a valid student ID. If you have pre-registered, your name badge and Technical Program will be ready for you to pick up at the registration desk during the conference. Please wear your name badge throughout the conference. Access will be prohibited to the exhibition, tea break, interactive areas, and technical sessions if a name badge is not visible.

Conference Registration Categories	Early Bird (Paid in full by Nov. 15)	Regular Registration (Paid after Nov. 15)
IEEE Member		
Full Member	USD 450 / RMB 3000	USD 500 / RMB 3300
Student Member	USD 250 / RMB 1700	USD 300 / RMB 2000
Life Member	Free	Free
Non IEEE Member		
Regular Registration	USD 490 / RMB 3300	USD 540 / RMB 3600
Student Registration	USD 270 / RMB 1800	USD 320 / RMB 2100

Guidelines for Presentation

Information for Oral Presenters:

Presenters are required to report at their session room to their session chair at least 15 minutes prior to the beginning of their session. Presenters are suggested to try out their presentations if there is any concern about the format, presentation length, etc. It is mandatory that the presentations should be loaded to the computer supplied by conference ahead of the beginning of each section. Any delays in the start of the presentation behind schedule due to the presenter's disregard of this guidance will result in less presentation time for that paper. All regular presentations are limited to 20 minutes (invited presentations will have 30 minutes). The strict limits are 15 minutes for formal presentations and 5 minutes for questions and discussions. To accommodate attendees who move between sessions, it is important to carry out every presentation on schedule. The Session Chair will remind the presenter 10 minutes after the presentation starts. The session room will be equipped with a computer and an LCD projector. This is the only permissible projection system. Presenter MUST use the session's computer for their presentation, i.e, their presentation must be loaded in advance on this computer.

Each computer is equipped with a CD-ROM drive and a USB port to read CDs and USB flash memory, respectively. The operation system for section computers is Microsoft Windows 7(or newer). The software available on each machines are Adobe Acrobat Reader (for PDF), Math Type and Microsoft Office (Version: Office 2013) with Word, Excel and Power Point Available. Therefore, all presenters must be compatible with these packages. There will be also assistance and advice available to presenters at registration desk. Please remember that due to the very large number of papers and a tight schedule, the responsibility of having your paper ready for presentation at the scheduled time is very important.

Information for Poster Session Presentations

Presenters are required to put up their papers 15 minutes prior to the beginning of their session. Each poster presentation will last about 50 minutes. During this time, the presenter must stand by the display board to answer questions and discuss about the contents of the poster informally. The poster display should include a statement the topic, objectives of the research project, the methodology used to solve the problem or implement the program, the major findings or outcomes and their significance and conclusions. There should be a logical sequence---- introduction, development and conclusion--- of your display.

Each sheet should numbered, a heading should be prepared for your presentation using lettering at least 3 cm high. The heading should include the title of the poster, all author names and institutional affiliations.

One poster board is provided for each presentation, which is 1.2 meter high by 0.8 meter wide. The back ground color of the board is usually beige or white. Pins or tapes are provided by conference committee to mount your posters on the boards. All materials to be displayed should be prepared before your arrival. Supplies will not be available at the conference site.

General Information

■ Projection Facilities

Standard LCD projector (connected to a local PC) will be provided in each conference room.

■ Conference Venue

EDAPS 2017 will be held at the Multimedia Hall of the international campus, Zhejiang University, in Haining, Hangzhou, CHINA.

For more information about the international campus, Zhejiang University, please visit the website http://www.intl.zju.edu.cn/.

For flights

- **Hangzhou Xiaoshan Airport (HGH)**
  Shuttle Bus : HGH Airport – Haining Coach Station
  Tickets&Waiting at Gate 14, Domestic Arrival Hall
- **Shanghai Hongqiao Airport (SHA)**
  High Speed Railway: Shanghai Hongqiao –Tongxiang Station
  Take a taxi or take No.188 Bus to the Terminal Station(Haining Coach Center).
- **Shanghai Pudong Airport (PVG)**
  Shuttle Bus: PVG Airport – Shanghai South Railway Station
  Regular Train: to Haining (海宁) Station

For trains

- **Haining Railway Station** (Regular Railway)
  *Notice: Hainingxi(海宁西)Railway Station is different from Haining (海宁) Railway Station, please don’t choose Hainingxi.
- **Tongxiang Railway Station** (High Speed Railway)

For buses

No.	Departure–Terminal	Time	Interval(Mins)	Stop
15	Coach station–Shooting hall	6:00–18:30	15–20	Leather Market, TV & Radio Center, food grocery, Material and child hygiene etc.
33	Intl campus–TrainStation	6:20–18:10	15–20	Train station, tax bureau, TV & Radio Center, Transportation Building, Social insurance center etc.
933	Intl Campus–CoachStation	18:30–21:00	30–40	Coach station, yintai mall, Haining hospital, book market, Social insurance center etc.
202	Train Station–Shidun county	6:30–17:50	50	Train station, Haining museum, Material and child hygiene etc.
29	Intl Campus– Xinguang County	6:20–18:20	10–15	Yintai mall, Haining hospital, Financial center, etc.

Tips

- **To taxi driver**
  我要去海宁市，浙江大学国际校区西门，海宁市硖石街道竞芳路，谢谢！
  I would like to go to the south gate of International Campus, Zhejiang University, Haining, which is Jingfang Road, Xiashi District, Thank you!
- **To security at the south gate of campus**
  我是来参加国际学术会议的，请让司机通行，把我载到校区圆正酒店
  I am here for attending IEEE EDAPS, please tell the taxi driver to drop me off at Yuanzheng Hotel.
- **Navigation**
  Search “Zhejiang University Haining International Campus” to navigation.
- **Official Address:**
  718 East Haizhou Road, Haining, 314400, Zhejiang Province, China (浙江省海宁市海州东路718号)
- **Coordinator:**

Ning Cheng(宁成)
Tel: +86 13216196625
Email: 21531021@zju.edu.cn

Xinran Zhu (朱欣然)
Tel: +86 15068954668
Email: xinranzhu@intl.zju.edu.cn

It’s recommended to activate the International calling in your cellphone.

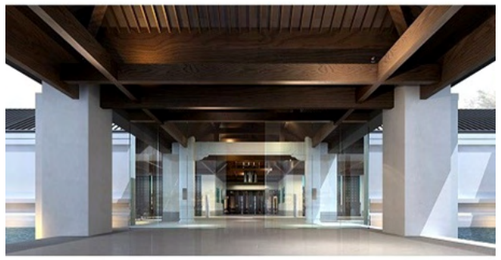
■ Accommodation

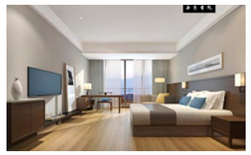
Yuanzheng hotel (5 Star Hotel)

The Yuanzheng hotel is holding a block of rooms at special rates for conference attendees. Room reservations must be made by December 13, 2017 to guarantee the accommodation.

ADD：NO.718 East Haizhou Road,
Haining, Zhejiang, China (In the ZJU-UIUC Campus)
浙江海宁海州东路 718 号
Tel: +86-0573-89706678, +86-0573-89706698,
+86-13095609911
Fax: +86-0573-89706696
Email: yuanzhengaikaite@sina.com

Phone bookings must be confirmed in written. Please send the reservation confirmation file to the Email address (yuanzhengaikaite@sina.com) for reservation.

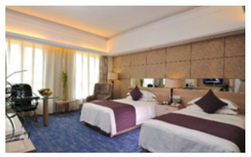




Haizhou hotel (5 Star Hotel)

The Haizhou Hotel is holding a block of rooms at special rates for conference attendees. Room reservations must be made by November 20, 2017 to guarantee the accommodation.

ADD：NO.199 Haizhou Road,
Haining, Zhejiang,China (7km. from the ZJU-UIUC Campus),
浙江海宁海州路 199 号
Tel: 0573-87288888
Fax: 0573-87289555
Email: hotel@haizhouhotel.cn
Http://www.haizhouhotel.cn


■ About Hangzhou

Hangzhou is the capital and most populous city of Zhejiang Province in east China. It sits at the head of Hangzhou Bay, which separates Shanghai and Ningbo. Hangzhou grew to prominence as the southern terminus of the Grand Canal and has been one of the most renowned and prosperous cities in China for much of the last millennium. The city's West Lake, is amongst its best-known attraction.

■ Qiantang Tide (Haining)

The Yanguan Tidal Bore Wacthing Scenic Spot, located at the strong tidal wave section of the Qiantang River, is the best place for enjoying this world marvel.

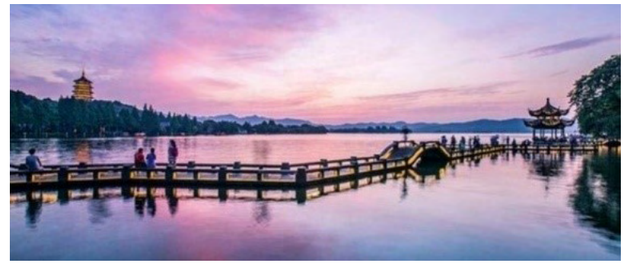
■ West Lake Cultural Landscape of Hangzhou

Lying in Hangzhou City of Zhejiang Province, the West Lake is a world famous tourist spot. Embraced by green hill on three sides. The whole lake is divided into 5 sections, namely the Outer Lake, North Inner Lake, WestInner lake, Yue Lake and Little South Lake, by Gu hill, Sudi Causeway, Baiti Causeway and Ruangong Mound. The beauty of the West Lake lies in its lingering charm that survives the changes of seasons in a year and of hours in a day.

■ Language

The official language of the conference is English. However in the public society, Chinese Mandarin is commonly spoken in Hangzhou.



■ Visa

Each person from abroad, who wants to enter the Chinese Customs, needs to hold a visa issued by Chinese Embassy or Consulate. It should be submitted to the Chinese Embassy in your country for you to apply for the visa. You can also apply for a visa type of common tourist, which is convenient to be issued without the requisition form and valid for 30 days.

■ Currency and Credit Cards

China's currency is RMB with its monetary unit RMB Yuan. The exchange rate is about 1 USD for 6.61 RMB. Only RMB cash is acceptable on the registration desk on the conference site. This is also the case in most large shopping centers and other hotels.

■ Tax and Tip

All the shopping is free of tax. Be sure to make big bargaining when buy merchandise from the Street Market. Tipping is by no means a tradition Chinese custom. Please help keep the good customs and do not tip a waiter/waitress or a taxi driver and other person who provides regular services.

■ Opening Hours

Bank and Post office opening hours: 9:00 a.m. to 5:00 p.m., from Monday to Sunday.

Government Office Opening hours: 8:00 a.m. to 5:00 p.m., from Monday to Friday.

Store Opening hours: 9:00 a.m. to 8:00 p.m., but the large shopping center serves till 10:00 pm., from Monday to Sunday.

■ Electricity

In China, the standard outlets provide AC of 220 V/50 Hz.

■ Taxi

Usually, a taxi is available along the roadsides, while you wave for it. However, at main streets it is only available at taxi stops and in front of the hotel

■ Internet Access

There are WLAN with internet access in the conference venue. Network Name: ZJUWLAN

Account: hellozjui Password: zjui.123

■ Edpas2017 Online

Information on EDPAS 2107 has been posted on the World Web at: http://www.edaps2017.org/detail.php?id=5

Keynote Presentation-1

Dec 14(Thu), 2017, 09:15-10:00
Multimedia Hall

Stochastic Electromagnetic Field Modeling for EMI/ EMC-Aware Design of Electronic Systems

Andreas C. Cangellaris
University of Illinois at Urbana-Champaign
cangella@illinois.edu

Abstract of the talk

Statistical electromagnetic field theory has been an integral part of the design of electromagnetically compatible electronic systems for many years. Structural and material complexity of the environment in which electromagnetic fields and wave phenomena must be considered and analyzed has traditionally been—and continues to be—the primary reason for the need of probabilistic approaches to their analysis. More recently, the impact of variability in the geometric attributes of the electronics and in the electromagnetic properties of materials has motivated a more extensive application of stochastic modeling and simulation in support of signal and power integrity analysis. The need for such analysis is further compounded by the uncertainty in layout and placement that is present throughout the design and, currently, is rarely taken into consideration in predictive electrical performance analysis.

Through the examination of some notable and promising ideas presented to date this talk will explore this emerging frontier in stochastic electromagnetic field modeling for EMI/EMC-aware analysis and design of electronic systems. From new mathematical and numerical methods for fast stochastic analysis, to machine learning methods, to the exploitation of properties of random matrices, this presentation will argue that the design automation community is presented with a significant arsenal of approaches and tools that can be used to advance the way EMI/EMC analysis and design of complex electronic systems is practiced.

Andreas Cangellaris

Andreas Cangellaris is the Dean of the College of Engineering and the M.E. Van Valkenburg Professor of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received his B.S. in Electrical Engineering from the Aristotle University of Thessaloniki, Greece in 1981, and his M.S. and Ph.D. degrees in Electrical Engineering from the University of California, Berkeley, in 1983 and 1985, respectively. His teaching and research interests span the areas of theoretical and applied electromagnetism, computational science and engineering, and methodologies and tools for electronic design automation with primary focus on noise-aware design of integrated electronic components, circuits and systems.

Professor Cangellaris is Fellow of IEEE. In 2005 he received the Alexander von Humboldt Research Award from the Alexander von Humboldt Foundation, Germany. He was an IEEE Microwave Theory & Techniques Distinguished Lecturer from 2008 to 2010. He is the recipient of the U.S. Army Research Laboratory Director's Coin in recognition of his outstanding performance on the Multidisciplinary University Research Initiative project on Standoff Inverse Analysis and Manipulation of Electronic Systems. In 2012, he was recognized by the IEEE Microwave Theory & Techniques Society with the IEEE Microwave Theory & Techniques Distinguished Educator Award.

Keynote Presentation-2

Dec 14(Thu), 2017, 10:30-11:15
Multimedia Hall

2D Materials for Smart Life

Kaustav Banerjee
University of California, Santa Barbara
kaustav@ece.ucsb.edu

Abstract of the talk

I will highlight the prospects of 2D materials for innovating energy-efficient transistors, sensors, and interconnects targeted for next-generation electronics needed to support the emerging paradigm of Internet of Everything. More specifically, I will bring forward applications uniquely enabled by 2D materials and their heterostructures that have been demonstrated in my lab for realizing ultra-energy-efficient electronics. This will include the world's first 2D-material channel band-to-band tunneling transistor that overcomes a fundamental power consumption challenge in all electronic devices since the invention of the first transistor in 1947, as well as a breakthrough interconnect technology based on doped-graphene-nanoribbons, which overcomes the fundamental limitations of conventional metals and provides an attractive pathway toward a low-power and highly reliable interconnect technology for next-generation integrated circuits. I will also bring forward a new class of ultra-sensitive and low-power sensors as well as area-efficient and high-performance passive devices, both enabled by 2D materials, for ubiquitous sensing and connectivity to improve quality of life.

Kaustav Banerjee

ProfessorKaustavBanerjeefromUC Santa Barbara is one of the world's leading innovators in the field ofnanoelectronics. His current research focuses on the physics, technology, andapplications of 2D nanomaterials and their heterostructures for designingnext-generation green electronics, photonics, and bioelectronics. Initiallytrained as a physicist, he graduated from UC Berkeley with a PhD in electricalengineering in 1999. A Fellow of IEEE, APS, and AAAS, Professor Banerjee hasmade seminal contributions toward extending the frontiers of energy-efficientelectronics. This includes pioneering work on 3D ICs, now being widelycommercialized, which has been recognized by IEEE with the 2015 Kiyo TomiyasuAward, one of the institute's highest honors. Professor Banerjee's radicalinnovations with 2D materials are setting the stage for a new generation ofultra-energy-efficient electronics needed to support the "Internet of Things".This comprised of demonstrating the world's first 2D-material based tunnelingtransistor that reduces power dissipation by over 90% (Nature 2015), as well asa novel energy-efficient interconnect technology based on graphene that alsoovercomes a fundamental reliability limitation of conventional interconnectmaterials (Nano Letters 2016).

Keynote Presentation-3

Dec 14(Thu), 2017, 11:15-12:00
Multimedia Hall

Integrating thermal, electrical, and materials issues for extreme-density power electronics

Philip Krein
Zhejiang University International Campus, Haining, Zhejiang, China
zikrein@zju.edu.cn

Abstract of the talk

Researchers today seek to increase the density of power electronic systems. If power management capability, measured in terms of watts per cubic centimeter, can rise by two or three orders of magnitude compared to the state of the art, applications will expand by similar amounts. Sophisticated power management and control are essential for electric transportation, renewable energy, medical implants, high-performance robotics, portable devices, and intelligent loads and infrastructure. Wide bandgap materials, including GaN and SiC, are examples of new materials that help support extreme advances. Dramatic increases in power density require thermal, electrical, and materials challenges to be considered co-equally at a systems level. This presentation describes scientific advances and challenges related to comprehensive integration of extreme density power electronics. Concepts such as thermal diodes and thermal switches support wide bandgap materials to offer novel tradeoffs and future promise. Applications that impose ambient temperatures above 200°C are given as an example. This brings power electronics into domains such as active engine actuation in jet aircraft, downhole drilling and control, and others. The discussion is linked to the work of the new U.S. National Science Foundation Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS).

Philip Krein

Philip Krein holds a PhD from the University of Illinois atUrbana-Champaign. He is Executive Dean at the Zhejiang University / Universityof Illinois at Urbana-Champaign Institute for engineering on the new ZhejiangUniversity International Campus in Haining, and also holds the GraingerEmeritus Chair in Electric Machinery and Electromechanics at the University ofIllinois. His research areas include power electronics, electric machines,electric transportation, and renewable energy.

Keynote Presentation-4

Dec 15(Fri), 2017, 08:00-08:45
Multimedia Hall

3D-IC Technology: Reliability Challenges and Biomedical Application

Tetsu Tanaka
Tohoku University, Aoba-ku, Sendai 980-8579, Japan
ttanaka@bme.tohoku.ac.jp

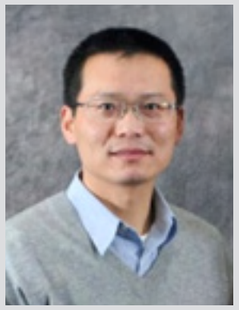
Abstract of the talk

3D-IC using TSVs is one of the most promising candidates for high performance computing system since 3D-ICs have lots of advantages such as high memory bandwidth and low power consumption due to short wiring length and small pin capacitances. Until now, several kinds of 3D-ICs including 3D-memory and 3D-CIS have been fabricated successfully. However, several reliability issues still remain in 3D-ICs with TSVs. In general, there are millions of TSVs and metal microbumps in vertically-stacked thinned Si chips. Both TSVs and metal microbumps cause local mechanical stress and strain in the Si chips due to coefficient of thermal expansion (CTE) mismatch between Si and Cu TSV and metal microbump. As the thickness of Si chip is less than several tens of μm, both intrinsic and extrinsic gettering layers to suppress metal contaminations and crystal defects might be eliminated from the Si chip by thinning process. This paper focuses on the 3D-IC reliability issues such as thermomechanical stress and Cu contamination, and presents effective evaluation methods for the issues. Moreover, several kinds of biomedical applications using 3D-IC and 3D integration technology are briefly presented.

Tetsu Tanaka

Tetsu Tanaka received the B.S. and M.S. degrees in electronics engineering and the Ph.D. degree in machine intelligence and systems engineering from Tohoku University, Sendai, Japan, in 1987, 1990, and 2003, respectively. In 1990, he joined Fujitsu Laboratories, Ltd., where he was engaged in the research and development of the highly- scaled MOSFETs including SOI devices. From 1994 to 1995, he was a Visiting Fellow with University of California, Berkeley. In 2005, he joined the Tohoku University as an Associate Professor, and became a Professor of Graduate School of Biomedical Engineering, Tohoku University in 2008. After joining Tohoku University, he is working on the research and development of integrated biomedical micro/nano-devices and systems using 3D-IC technology and neural engineering. His current research topics include fully-implantable retinal prosthesis, intelligent Si neural probe, 3D integration technology, and analog/digital IC design. He has published more than 150 technical papers and given more than 30 invited talks. He has or had served as a technical committee member or an editor of various international conferences and journals, such as International Technology Roadmap for Semiconductors (ITRS, 2006-2016), International Interconnect Technology Conference (IITC, 2008-), International Conference on Solid State Devices and Materials (SSDM, 2008-), Symposium on VLSI Technology (2009-), International Electron Devices Meeting (IEDM, 2011-2012), and Japanese Journal of Applied Physics (JJAP, 2009-2011).

Keynote Presentation-5



Dec 14(Thu), 2017, 09:15-10:00
Multimedia Hall

Signal Integrity Designs of HBM in 3D Packaging

Jun Fan
Missouri University of Science and Technology,
Rolla, MO 65409, USA.
jfan@mst.edu

Abstract of the talk

High-bandwidth memory (HBM) is a high-performance memory interface to achieve high bandwidth, low power dissipation, and advanced packaging, which uses more than a thousand channels. This number is more than 10 times increased compared to the conventional DDR memory, and 3D packaging solutions may be required for the dense signal routing. Because of these unique features/requirements of HBM, there exist several new challenges including high DC loss, large crosstalk even for shorter lengths of channels, and large power noise due to the switching of thousands of I/O drivers. These problems can affect the received signal quality and reduce the timing margin, resulting in potential system failures. In this talk, signal integrity designs in a typical HBM application are discussed, including the packaging choice between silicon interposer and EMIB, trace routing density and type, crosstalk estimation, and power supply induced jitter. A statistical eye-diagram estimation method is presented to design and evaluate the HBM channels including both signal and power nets. Several types of HBM transmission lines are compared in terms of insertion loss, characteristic impedance, and required number of routing layers. PDN is modeled using lumped elements, and I/O driver is assumed as an inverter using the 180nm MOS technology. Because of the difficulties of low BER simulation at SPICE, a multiple edge response (MER) based method is used to obtain the statistical eye-diagram at the receiver. Data Bus Inversion (DBI) coding is handled in this statistical method.

Jun Fan

Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a Professor and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009.

Tutorial – I

Dec 14(Thu), 2017, 13:30-14:30
201, Lecture Theatre West

High-Speed Circuit Modeling and Design Using X Parameters

Organizer and Speaker: Prof. Jose Schutt-Aine
University of Illinois, Urbana, USA
jesa@illinois.edu

Abstract of the talk

The era of big data will lead to systems handling the transport of large amounts of information. Simulation techniques for the prediction of signal propagation in these environments have become a subject of increased interest over the past few years. Behavioral and macro-modeling techniques have been among the most popular methods used to predict the performance of these systems. Currently, IBIS model interpreters/generators are used to achieve a behavioral representation of nonlinear circuit blocks from their ports. However, when switching speeds increase, these models are no longer accurate.

The introduction of X parameters* has created new possibilities for the analysis of nonlinear behavior in high-speed circuits. The concurrent introduction of nonlinear vector network analyzers (NVNA) has reinforced the viability of the technique. X parameters represent a superset of the traditional scattering parameters and offer a mathematical foundation for the treatment on nonlinear network and components. This introduction presents a serious opportunity for the modeling and analysis of serial links.

In this tutorial, we review the fundamentals of X parameters as the nonlinear superset of S parameters and discuss techniques to generate the time-domain response of high-speed links. X parameters are first obtained in the frequency domain. We address the issues related to the steady-state simulation before looking into transient behavior. In particular, we explore the problem of Volterra series representation combined with machine learning techniques to construct powerful mathematical models for nonlinear circuits. A comparative study of different approaches and results is also given.

José E. Schutt-Ainé

José E. Schutt-Ainé received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1981, and the M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign (UIUC), Urbana, in 1984 and 1988, respectively. From 1981 to 1983, he worked at the Hewlett-Packard Technology Center, Santa Rosa, CA, as an Application Engineer, where he was involved in research on microwave transistors and high-frequency circuits. In 1988, he joined the Electrical and Computer Engineering Department as a member of the Electromagnetics and Coordinated Science Laboratories, where he is currently involved in research on signal integrity for high-speed digital and high-frequency applications. He is a consultant for several corporations. His current research interests include the study of signal integrity and the generation of computer-aided design tools for high-speed digital systems. Dr. Schutt-Ainé was a recipient of several research awards, including the 1991 National Science Foundation (NSF) MRI Award, the NASA Faculty Award for Research in 1992, the NSF MCAA Award in 1996, and the UIUC-NCSA Faculty Fellow Award in 2000. He has received several publication awards including the IEEE EDAPS- 2013 Best Paper and the IEEE-EPEPS-2014 Best Paper. He is an IEEE Fellow and is currently serving as Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT).

*X-Parameters is a Trademark of Keysight Technologies, Inc.

Tutorial – II

Achieving Power Integrity through a Systematic Physics-Based Design
Organizer: Prof. James L. Drewniak
Missouri University of Science and Technology, USA
drewniak@mst.edu

Dec 14(Thu), 2017, 13:30-14:00
204, Lecture Theatre West

Topic 1: Power Integrity Concepts for Physics-based PDN Design

Speaker: Prof. James L. Drewniak
Missouri University of Science and Technology, USA
drewniak@mst.edu

Abstract of the talk

Power integrity in high-speed digital designs is among the significant design challenges for high data rate and high speed systems. Best engineering practices for design of a power distribution network at the package and PCB level are well known. In practice this comes down to minimizing inductance over the current-draw path. However, there are many subtle design choices that can impact achieving a minimal power net voltage ripple or meeting a target impedance specification. In order to achieve a best design with or without constraints on some of these choices, a proven methodology for calculating the portions of inductance associated with particular geometry features is necessary, and a knowledge of inductance physics that can be exploited to achieve the design specification within a given stackup and a minimal number of decoupling capacitors.

A systematic methodology has been developed for PDN design and PI analysis that can readily identify a best design given typical design constraints. A method for PDN impedance calculation will be shown, and approach for achieving a target impedance will be given. If the target impedance specification is not met, the developed methodology can be used to immediately identify if specifications can be met with design modifications within the constraints, and provide directions in doing so in one or two iterations while avoiding trial-and-error simulations.

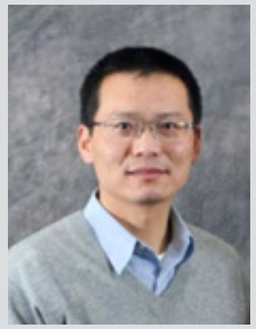
James L. Drewniak

James L. Drewniak is a Curator's Professor of Electrical and Computer Engineering at Missouri S&T. He received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign. His research is in electromagnetic compatibility, signal and power integrity, and electronic packaging. He is with the Electromagnetic Compatibility Laboratory, a university research laboratory of approximately 70 people that is internationally recognized for research in EMC and signal and power integrity. A key component of the research funding is the NSF Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility that is a consortium of approximately 20 companies. He is a Fellow of the IEEE, 2013 recipient of the IEEE EMC Society's Richard R. Stoddart Award, and a past Associate Editor of the IEEE Transactions on EMC.

Dec 14(Thu), 2017, 14:00-14:30
204, Lecture Theatre West

Topic 2: A Pre-layout Design Approach for Achieving a Target Impedance

Speaker: Prof. Jun Fan
Missouri University of Science and Technology,
Rolla, MO 65409, USA.
jfan@mst.edu



Jun Fan

Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a Professor and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009.

Dec 14(Thu), 2017, 14:30-15:00
204, Lecture Theatre West

Topic 3: Low Inductance Decoupling Capacitor Interconnects and Library Models

Speaker: Prof. Er-Ping Li
Zhejiang University
liep@zju.edu.cn

Li Er-Ping

Li Er-Ping is currently a Changjiang-Qianren Distinguished Professor, Dean of ZJU-UIUC Institute (Zhejiang University-University of Illinois at Urbana-Champaign), China. Prior that, he held various academic and managerial positions, he was the Department Director and Senior Director at A*STAR Institute of High Performance Computing, Deputy Dean to Faculty of Information Technology, Zhejiang University. He also served as Adjunct Associate Professor to ECE NUS from 2002-2008, Adjunct Professor to Peking University, Adjunct Professor at Applied Physics at NTU from 2012 to 2014. Dr Li served the Global Advisory Panel to KAIST and External Academic Panel to City University of Hong Kong. Dr. Li is pioneering in applied electromagnetics and high speed electronics, he authored or co-authored over 400 papers published in the referred international journals and conferences, authored two books published by John-Wiley-IEEE Press and Cambridge University Press, holds and has filed a number of patents at the US patent office. He has been invited to give over 80 invited and keynote speeches at various international conferences and forums.

Dec 14 (Thu), 2017, 15:00-15:30
204, Lecture Theatre West

Topic 4: Calculating Time-Domain Noise Voltage for Power Integrity

Speaker: Prof. James L. Drewniak
Missouri University of Science and Technology, USA
drewniak@mst.edu

James L. Drewniak

James L. Drewniak is a Curator's Professor of Electrical and Computer Engineering at Missouri S&T. He received B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois at Urbana-Champaign. His research is in electromagnetic compatibility, signal and power integrity, and electronic packaging. He is with the Electromagnetic Compatibility Laboratory, a university research laboratory of approximately 70 people that is internationally recognized for research in EMC and signal and power integrity. A key component of the research funding is the NSF Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility that is a consortium of approximately 20 companies. He is a Fellow of the IEEE, 2013 recipient of the IEEE EMC Society's Richard R. Stoddart Award, and a past Associate Editor of the IEEE Transactions on EMC.

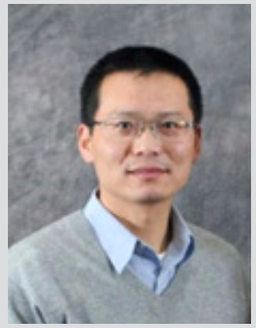
Tutorial – III

Interconnect Characterization and IPC D24D Standard Development
Organizers: Prof. Jun Fan and Dr. Xiaoning Ye
Missouri University of Science and Technology, USA
jfan@mst.edu

Dec 14(Thu), 2017, 15:50-16:20
204, Lecture Theatre West

Topic 1: PCB Material Characterization for High-Speed Interconnect Modeling

Speaker: Prof. Jun Fan
Missouri University of Science and Technology,
Rolla, MO 65409, USA.
jfan@mst.edu



Abstract of the talk

This talk introduces the latest progress in characterizing the material properties in fabricated multi-layer printed circuit boards, taking into account the effects of test fixtures, conductor surface roughness and the frequency-dependent behaviors of the board materials. Methodologies and tools are presented to facilitate engineers to achieve accurate material characterization necessary for modeling PCB channels at higher speeds. Practical issues are discussed with real-world examples.

Jun Fan

Jun Fan received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a Professor and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009.

Dec 14(Thu), 2017, 16:20-16:50
204, Lecture Theatre West

Topic 2: IPC D24D Development for Accurate PCB Characterization

Speaker: Dr. Xiaoning Ye
Intel Corporation, USA
xiaoning.ye@intel.com

Abstract of the talk

The data rates of high-speed differential serial links have grown exponentially over the last two decades to meet ever-increasing bandwidth requirements. In light of these increasing data rates, controlling and measuring properties of printed-circuit-boards (PCBs) are now crucial components of high speed interconnect design. There are several factors that contribute to PCB trace transmission line loss, which include material properties (loss tangent of laminate, copper conductivity, copper foil surface roughness, etc.), all of which may change during the manufacturing process. As a result, direct measurement of fabricated PCB trace is always necessary nowadays.

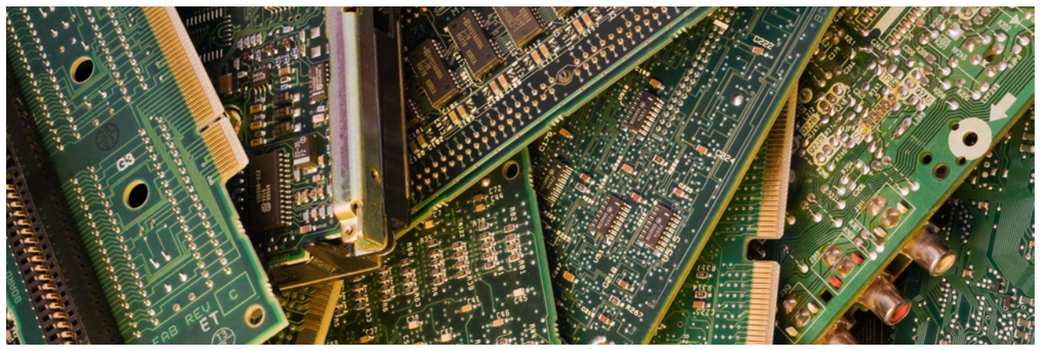
Traditional PCB test methods are hard pressed to keep up with the demanding requirements for high data rates and measurement accuracy. However, most of the IPC test methods are based on TDR/TDT measurements, and the test fixtures and PCB via impact are not properly addressed for accurate PCB transmission line characterization. Current IPC test methods under TM-650 are not adequate to address the quality of measured data for electrical printed boards to meet the demand of high speed applications. Furthermore, current IPC standard does not encompass common industry methods (such as TRL, etc.) and new/recent developments of 2X-thru method (such as AFR*, SFD* approach, etc.)

Intel DCG (DataCenter Group) Engineering Team has been working with Industry Partners to address this issue for several years, including the introduction of Delta-L and Delta-L+ approach. Initiated and led by Intel engineers, IPC D24D task-force was established in 2016 to close the gap in the existing standard. In this talk, we will report recent progress of D24D task force, including:

- Calibration/De-embedding techniques
- Test fixture quality requirements
- Foot print optimization for probing
- Validation of Measurement data
- Temperature/Humidity impact, etc.

Xiaoning Ye

Xiaoning Ye received the Bachelor's and Master's degrees from Tsinghua University, Beijing, China, in 1995 and 1997, respectively, and the Ph.D. degree from the University of Missouri-Rolla (currently Missouri University of Science and Technology), Rolla, in 2000, all in electrical engineering. Dr. Ye joined Intel Corporation in 2001, and he is currently a Principal Engineer in Data Center Group, responsible for signal integrity of high speed interconnect. Dr. Ye holds eight patents and a few more patent applications in the areas of high-speed signaling. He is currently Vice Chair of the IEEE EMC Society Technical Advisory Committee, and Associate Editor of IEEE Transaction on EMC.



Dec 14(Thu), 16:50-17:20
204, Lecture Theatre West

Topic 3: Robust Probe Design and Unified Probe Pad for PCB Measurements

Speaker: Dr. Richard Zai
Packet Micro, USA
rzai@packetmicro.com

Abstract of the talk

Microprobes are commonly used for PCB interconnect measurement. Although they are suitable for accurate measurements in laboratory settings, they are often too fragile for high-volume testing. This talk presents a robust probe design, which is suitable for PCB measurements up to 20 GHz. The probe is mechanically stronger and can be used for handheld measurements. In addition, a unified probe pad design is suggested. Simulations are presented to demonstrate the effectiveness of the pad design. The unified probe pad design could facilitate the standard work for PCB characterization.

Dr. Richard Zai

Dr. Richard Zai is Packet Micro CTO and has more than 25 years of experience in architecting and delivering technology solutions in the areas of RF and signal integrity probing, wireless sensor networks, and radio frequency identification (RFID). In 1987, he joined IBM Watson Research Center as a research staff member and manager, where he pioneered in the development of RFID and high-speed robotic technologies. After leaving IBM in 1997, Richard co-founded start-up companies in Silicon Valley. Most recently, he has been leading the development of rugged 20-GHz test probes and patented probe stations that have been used by many Fortune 100 companies. Richard receives his Ph.D. degree from the University of Wisconsin-Madison and holds 15 US patents.

Dec 14(Thu), 2017, 17:20-17:50
204, Lecture Theatre West

Topic 4: Interconnect Characterization to Support Future Generation of High-Speed I/O

Speaker: Dr. Chunfei Ye
Intel Corporation, USA
Chunfei.ye@intel.com

Abstract of the talk

With the ever increasing IO data rate, interconnect characterization becomes critical for link design. Modeling, measurement, correlation and specification are among the key efforts for interconnect characterization. This talk covers characterization of PCB, cable and other components by addressing challenges and possible solutions.

Dr. Chunfei Ye

Dr. Chunfei Ye obtained B. Sci. in Mathematics from Hangzhou University in 1982, M. Eng from China Research Institute of Radiowave Propagation in 1985 and Doctoral Degree of Engineering in 1994 from Southeast University, both in EE. Before joining Intel China in 2002 as signal integrity (SI) and power integrity (PI) manager, Dr. Ye worked as a researcher with Shanghai Tiedao University, China, Institute of High Performance Computing, Singapore, and Massachusetts Institute of Technology, etc. He has been working with Intel Data Center Group since 2005 as SI tech lead, supporting all generations of Intel server PCH and SOC CPU package and platform signal integrity design. Dr. Ye serves as IEEE EMC-S TC 10 (SI and PI) Vice Chair and IEEE EMC-S Distinguished Lecturer 2016-2017. He has published more than 50 papers on international conferences and journals and was granted 3 US patents.

Dec 14(Thu), 2017, 17:50-18:20
204, Lecture Theatre West

Topic 5: Temperature Impact on Printed Circuit Board (PCB) Transmission Line Loss

Speaker: Mr. Jimmy Hsu
Intel Corporation
jimmy.hsu@intel.com

Abstract of the talk

Channel loss is a dominant factor for the signaling performance of high-speed application and how to evaluate the temperature impact on PCB loss is becoming more important. In this study, the best-known method (BKM) of temperature impact on PCB transmission line loss and design flow were proposed for signal integrity design. The material with less loss characteristics is less sensitive to the temperature change and different material has different temperature sensitive characteristics. The system designers need to check with PCB supplier and/or material vendor to understand the temperature impact of material of choice, and validate with simulation or measurement to evaluate this design risk.

Xiaoning Ye

Jimmy Hsu graduated from the electrical engineer department of national Chiao Tung University on 2000. He worked for Via technology from 2000 to 2008 and was in charge of SI/PI and EMI in Himax from 2008 to 2010. He joined Intel as data center signal integrity to enable customer and innovation technology development.

Workshop -I

PEEC Modeling for Signal Integrity and EMC Analysis
Organizer: Ke-Li Wu
The Chinese University of Hong Kong
klwu@ee.cuhk.edu.hk

Dec 14(Thu), 2017, 14:30-15:00
207, Lecture Theatre West

Topic 1: Circuit Oriented Electromagnetic Modeling Using the PEEC Techniques

Speakers: Albert E. Ruehli, Giulio Antonini and Lijun Jiang*
Missouri University of Science and Technology, Università degli Studi dell'Aquila, and University of Hong Kong*
ljiang@eee.hku.hk

Abstract of the talk

Electromagnetic (EM) modeling has been of interests to authors of this topic for a large portion of their careers. The PEEC method evolved in a time span of more than 40 years. From the start, the approach has been tailored for electromagnetic modeling of electronic packages or electronic interconnects, which are also called signal integrity (SI), power integrity (PI), noise integrity (NI), as well as EMC problems. In the beginning, only high-performance computer system modeling needed accurate models for the electrical performance of interconnects and power. Quasistatic solutions were adequate even for the highest performance systems. But very soon due to problems of the ever-increasing size, this work was further extended to partial inductance calculations. With the race for higher clock rates in computer chips, the modeling of higher performance chips and packages led to the need for full-wave solutions. As a consequence, stability and passivity issues became important. Today, aspects such as skin-effect loss and dielectric loss models are required for realistic analysis.

Electromagnetic physics-based PEEC equivalent circuit models can be constructed for a multitude of purposes. It has many intrinsic connections with modern computational electromagnetic (CEM) algorithms. PEEC has been conveniently used in practical SI/PI modeling processes to pin point troublemakers in the high-speed electronic system designs. It is also functioning as the physical extraction method underneath many EDA tools. In this tutorial, we will review the development trajectory of PEEC methods, major applications, and several frontier topics rooted in the PEEC idea.

Lijun Jiang

Dr. Lijun Jiang received the Bachelor Degree in electrical engineering from the Beijing University of Aeronautics and Astronautics in 1993, the Master Degree from the Tsinghua University in 1996, and the Ph.D from the University of Illinois at Urbana-Champaign (UIUC) in 2004. From 1996 to 1999, he was an Application Engineer with the Hewlett-Packard Company (HP). From 2004 to 2009, he has been the Postdoc, the Research Staff Member, and the Senior Engineer at IBM T.J. Watson Research Center. Since Dec. 2009, he has been the Associate Professor at the Department of Electrical and Electronic Engineering, the University of Hong Kong. He was the Senior Visiting Professor at Tsinghua University from Jun. 2013 to Jun. 2014. And he has been the visiting scholar to Professor T. Itoh's group at UCLA since Sept. 2014 and spent his Sabbatical at UCLA during Sept. 2014 to Mar. 2015.

Dec 14(Thu), 2017, 15:00-15:30
207, Lecture Theatre West

Topic 2: PEEC-Based Micro-Modeling Circuit for Signal Integrity – Its Theory, Algorithm, Passivity and Applications

Speakers: Yuhang Dou and Prof. Ke-Li Wu*
The Chinese University of Hong Kong
klwu@ee.cuhk.edu.hk

Abstract of the talk

This talk will present the basic concept and the application of a physically derived micro-modeling method for signal integrity analysis of large-scale high-speed and high-density interconnection problems. The micro-modeling circuit is an order-reduced circuit of the partial element equivalent circuit (PEEC) model that is formulated from MPIE and is constructed based on meshing information. The micro-modeling circuit can be obtained by absorbing the insignificant nodes of the PEEC model one by one recursively according to a physics-inspired equivalent circuit transformation and an approximation that retains the essence of the original circuit in a lowpass sense. The process of deriving the micro-modeling circuit doesn't involve any matrix inversion nor physically meaningless circuit components which warrants that the method will not suffer from the scalability problem in time-domain signal integrity analysis.

This talk will also present the mathematic rationale and strategy of using GPU parallel computation techniques for accelerating the micro-modeling. The passivity of the micro-modeling circuit is warranted by a new simple passivity enforcement method. Some practical interconnection examples will be given to demonstrate the versatility, scalability, accuracy, and the simplicity of the new micro-modeling method. It will be shown through numerical examples that the micro-modeling circuit can be three orders of magnitude faster than the traditional PEEC modeling in practical signal integrity analysis.

Ke-Li Wu

Ke-Li Wu has been with The Chinese University of Hong Kong since 1999, where he is a Professor of Dept. of Electronic Engineering and the Director of the Radiofrequency Radiation Research Laboratory. His current research interests include microwave filters, multiple antennas for wireless systems, EM modeling of signal integrity for high-speed packages, and technologies for Internet of Things.

Prof. Wu is a Fellow of IEEE, a member of IEEE MTT-8 subcommittee (Filters and Passive Components).

Dec 14(Thu), 2017, 15:50-16:20
207, Lecture Theatre West

Topic 3: Key Challenges in EMI/ESD Control for 5G Telecommunication Network Products

Speaker: Dr. Yao-Jiang Zhang
Huawei Technologies
zhang.yaojiang@huawei.com

Abstract of the talk

With the data rate increasing to tens Gbps, it becomes more and more difficult to reduce EM radiation from ICs, connectors and optical modules. Shielding by a chassis with ventilation holes is not enough to prevent electromagnetic energy leaking from the high-speed products. Novel measures have to be investigated to reduce EM radiations from integrated circuits, connectors, cables and/or optical modules. On the other hands, the feature size of ICs is continuously reduced to even 10/7nm. It becomes more and more difficult to balance component level electro-static discharge (ESD) protection and manufacture process. Besides hard failures, soft failures caused by ESD or electrical overstress (EOS) are more and more serious. Collaboration among several research areas, including ESD/EMI, signal integrity (SI) and power integrity (PI), is required to overcome these challenges.

Yao-Jiang Zhang

Yao-Jiang Zhang, IEEE Senior Member, received his B.E. and M. E. from University of Science and Technology of China in 1991 and 1994, respectively. In 1999, he got Ph.D. degree in Physical Electronics from Beijing University. From 1999 to 2001, he worked in Tsinghua University as a research fellow. From 2001 to 2014, he had worked as senior research engineer, research scientist, associate research professor in the Institute of High Performance Computing (IHPC), Agency for Science, Technology and Research (A*STAR), Singapore, and EMC Laboratory, Missouri University of Science & Technology, USA. From 2014, he is working in Huawei Technologies as a Chief EMC Expert and Director of electromagnetic engineering and protection Lab.

His research interests include computational electromagnetics, signal/power integrity issues in high-speed electronic packages and PCBs, passive inter-modulation in base-station antennas, antenna array design, electromagnetic compatibility and EM protection for telecommunication network products, and optical components, etc.

Dec 14(Thu), 2017, 16:20-17:20
207, Lecture Theatre West

Topic 4: The Concept of Radiation Resistance in Frequency-domain PEEC Model

Speakers: Chiu-Chih Chou and Prof. Tzong-Lin Wu
National Taiwan University
tlwu@ntu.edu.tw

Abstract of the talk

The traditional time-domain PEEC deals with real circuit elements (RLC) while some quantities are evaluated at the retarded time. The frequency-domain PEEC formulation eliminates the difficulty for the retarded time, but introduces complex inductance and potential coefficients whose physical meaning were studied in detail only recently. Several works together revealed that the imaginary parts of the mutually-coupled complex inductance and complex capacitance represent the radiation resistance network of the whole structure. In this talk, we will go through the development of the understanding regarding the meaning of complex LC. The relation between the imaginary LC and radiation resistance will be rigorously derived based on Poynting's theorem, and some physical implications of the result will be discussed.

Chiu-Chih Chou

Chiu-Chih Chou received the B.S.E.E. from National Taiwan University (NTU) in 2011. He is currently pursuing Ph.D. degree at the Graduate Institute of Communication Engineering, National Taiwan University. His research interests include EMC/SI/PI and applied electromagnetic.

Tzong-Lin Wu

Tzong-Lin Wu is a Fellow of IEEE. He received the B.S.E.E. and Ph.D. degrees from National Taiwan University (NTU), Taipei, Taiwan, in 1991 and 1995, respectively. From 1995 to 1996, he was a Senior Engineer with Microelectronics Technology Inc., Hsinchu, Taiwan. In 1996, he joined the Central Research Institute of the Tatung Company, Taipei, where he was involved in the analysis and measurement of EMC/EMI problems of high-speed digital systems. In 1998, he joined at the Electrical Engineering Department, National Sun Yat-sen University. Since 2006, he has been a Professor with the Department of Electrical Engineering, NTU. His current research interests include EMC/EMI and the signal/power integrity design for high-speed digital/optical systems. Dr. Wu is the recipient of many prestigious awards including the IEEE Transactions on Advanced Packaging Best Paper Award in 2011. He served as the Distinguished Lecturer with the IEEE EMC Society from 2008 to 2009. He is currently an Associate Editor of the IEEE Trans on EMC and the IEEE Trans. CPM

Dec 14(Thu), 2017, 17:20-17:50
207, Lecture Theatre West

Topic 5: An Effective PEEC Modeling Method to Solve System-level ESD Noise Problem

Speaker: Prof. Jingook Kim
Ulsan National Institute of Science and Technology
jingook@unist.ac.kr

Abstract of the talk

The coupling from electrostatic discharge (ESD) events can be effectively calculated using the partial element equivalent circuit (PEEC) method both in time and frequency domains. The PEEC method has several advantages in predicting dominant coupling sources and waveforms of ESD. First, the ESD generator can be easily incorporated as an equivalent circuit model in the PEEC method. Second, the PEEC method allows a fast and accurate calculation method of system-level ESD noise coupling based on the model decomposition process. The proposed method can significantly reduce the calculation time without loss of accuracy by separating small victim structures from the large aggressor structures such as ground planes and ESD gun strap. Also, when the overall aggressor geometry is fixed and the coupling to various victim geometries needs to be found, the separation of aggressor and victim structures reduces the computational time significantly. Using the method, the ESD noise coupling at the terminations of a victim signal trace is rigorously calculated and validated with measurements and full-wave simulations both in frequency and time domains.

Jingook Kim

Jingook Kim received his B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejon, Korea, in 2000, 2002, and 2006, respectively. From 2006 to 2008, he was with DRAM design team in Memory Division of Samsung Electronics, Hwasung, Korea, as a senior engineer. From January 2009 to July 2011, he worked for the EMC Laboratory at the Missouri University of Science and Technology, Missouri, USA, as a postdoc fellow. In July 2011, he joined the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, where he is currently an associate professor. He has authored or co-authored over 100 journal and conference papers. His current research interests include high-speed I/O circuits design, 3D-IC, EMC, ESD, RF interference

Dec 14(Thu), 2017, 17:50-18:20
207, Lecture Theatre West

Topic 6: PEEC Modeling for Lightning Protection, Magnetic Shielding and Transient Simulation

Speaker: Prof. Patrick Y. Du
The Hong Kong Polytechnic University
ya-ping.du@polyu.edu.hk

Abstract of the talk

With the proliferation of electrical and electronic systems, the electromagnetic (EM) environment in or around modern buildings, telecommunication facilities and other grounded structures has been increasingly concerned as the EM fields can cause interference to sensitive equipment and potential adverse health effects. The EM fields of concern in this presentation are mainly contributed by power equipment running at power frequency or a lightning protection system (LPS) during a lightning strike. The lightning protection system is intended to intercept lightning and to carry substantial lightning current. This current will generate intense transient electromagnetic fields in and around the grounded structure.

Many numerical methods have been developed to analyze electromagnetic compatibility problems which include MoM, FEM, FDTD and others. Recently, PEEC has been increasingly used in lightning transient analysis because its advantages in wire modelling. This method has been further extended to model planar structures as well for shielding analysis at low frequency. This presentation reports recent advances in PEEC applications for evaluating the electromagnetic environment in buildings caused by power-frequency equipment and lightning current, and lightning transients in radio bases stations. Modelling techniques for metallic structures found in buildings and steel towers are presented, which include steel bars, metal decking, metal trunking and other large metal plates or sheets. These metallic parts may not be part of electrical equipment or systems, but they do affect the electromagnetic environment in the buildings or at the towers. Examples are given to illustrate how these modelling techniques are applied to the electromagnetic environment evaluation, shielding effectiveness evaluation and lightning transient evaluation. A simulation tool TAES is introduced finally to analyze lightning transient currents in a cabling system for the radio base station.

Patrick Du

Patrick Du graduated with the Bachelor of Science in Electrical Engineering from Shanghai Jiao Tong University, and received the Doctor of Philosophy degree from the University of Southern California in the US. He joined the Hong Kong Polytechnic University in 1995 as an Assistant Professor, and is now a Professor in the Department of Building Services Engineering. His research interests include building electromagnetic environments, electromagnetic compatibility, and lightning protection for electrical distribution systems, railway systems, and communication systems. He serves as a consultant for local industry in the areas of electromagnetic compatibility and lightning protection. Currently he is a member of the Steering Committee of the Asia-Pacific International Conference on Lightning. He is a member of IET and a chartered engineer of the UK.

Workshop -II

Multiphysics Modeling and Simulation for Advanced Integration and Packaging
Organizers: Lijun Jiang, Gaobiao Xiao, and Jianming Jin
University of Hongkong, Shanghai Jiao Tong University, and University of Illinois
jianglj@hku.hk, gaobiaoxiao@sjtu.edu.cn, and j-jin1@illinois.edu

Dec 14(Thu), 2017, 16:20-16:50
201, Lecture Theatre West

Topic 1: Multiphysics modeling and simulation for large-scale integrated circuits

Speakers: Dr.Tianjian Lu and Prof. Jian-Ming Jin
University of Illinois at Urbana-Champaign,306 North Wright Street, Urbana, IL 61801, USA
j-jin1@illinois.edu

Abstract of the talk

This workshop presentation summarizes our efforts and findings in seeking solutions to two important and challenging problems related to the design of modern integrated circuits (ICs): the ever-increasing couplings among the multiphysics and the large problem size arising from the escalating complexity of the designs. A multiphysics-based computer-aided design methodology is proposed and implemented to address multiple aspects of a design simultaneously, which include electromagnetics, heat transfer, fluid dynamics, and structure mechanics. The multiphysics simulation is based on the finite element method for its unmatched capabilities in handling complicated geometries and material properties. The capability of the multiphysics simulation is demonstrated through its applications in a variety of important problems, including the static and dynamic IR-drop analyses of power distribution networks, the thermal-ware high-frequency characterization of through-silicon-via structures, the full-wave electromagnetic analysis of high-power RF/microwave circuits, the modeling and analysis of three-dimensional ICs with integrated microchannel cooling, the characterization of micro- and nanoscale electrical-mechanical systems, and the modeling of decoupling capacitor derating in the power integrity simulations. To perform the large-scale analysis in a highly efficient manner, a domain decomposition scheme, parallel computing, and an adaptive time-stepping scheme are incorporated into the proposed multiphysics simulation. Significant reduction in computation time is achieved through the two numerical schemes and the parallel computing with multiple processors.

Jian-Ming Jin

Jian-Ming Jin is Y. T. Lo Chair Professor in Electrical and Computer Engineering and Director of the Electromagnetics Laboratory and Center for Computational Electromagnetics at the University of Illinois at Urbana-Champaign. He has authored and co-authored over 275 papers in refereed journals and over 20 book chapters. He has also authored The Finite Element Method in Electromagnetics, Electromagnetic Analysis and Design in Magnetic Resonance Imaging, and Theory and Computation of Electromagnetic Fields, co-authored Computation of Special Functions, Finite Element Analysis of Antennas and Arrays, and Fast and Efficient Algorithms in Computational Electromagnetics. His name often appeared in the University of Illinois's List of Excellent Instructors. He was elected by ISI among world's most cited authors in 2002. He is a Fellow of IEEE, Applied Computational Electromagnetics Society (ACES), and Electromagnetics Academy. Recently, he received the 2014 ACES Technical Achievement Award, 2015 IEEE APS Chen-To Tai Distinguished Educator Award, 2016 ACES Computational Electromagnetics Award, and 2017 IEEE APS Harrington-Mittra Computational Electromagnetics Award.

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Topic 2: Coupled Thermo-electromagnetic Analysis Based on Integral Equations

Speakers: Gaobiao Xiao and Yibei Hou
Shanghai JiaoTong University
gaobiaoxiao@sjtu.edu.cn

Abstract of the talk

The power density handled in an electronic system has increased significantly in the past years, so does the leakage power. Leakage power may generate heat and cause high internal temperature in the device. The electronic device can be functionally deteriorated or even be damaged due to the high internal temperatures. Thermal management is an important issue for a compact electronic system, and thermo-electro- magnetic analysis may play a significant role.

There are many numerical techniques for analyzing this kind of heat transfer problems. The heat in an electronic system may be generated by ohmic loss in conductors and lossy media, switching loss in capacitances, etc. All these heat sources are dependent on current densities or electromagnetic fields that also have to be numerically calculated. In this workshop, we try to solve the coupled thermo-electromagnetic problem based on integral equations associated with the corresponding electromagnetic problem and the heat transfer problem. The equivalence source principle is used in the analysis of the electromagnetic scattering problem and the heat conduction problem. Based on the equivalence principle, integral equation formulations for electromagnetic scattering problems and steady-state heat analysis are introduced. Basically, the numerical implementation of solving the heat conduction equation can be embedded in the process of analyzing the corresponding electromagnetic problem. Therefore, it is possible to solve heat conduction problem and electromagnetic scattering problem with the same computer–code on a single mesh structure.

Gaobiao Xiao

Dr. Gaobiao Xiao received the M.S. degree from Huazhong University of Science and Technology, Wuhan, China, in 1988, the B.S. degree from the National University of Defense Technology, Changsha, China, in 1991, and the Ph.D. degree from Chiba University, Chiba, Japan, in 2002. He worked in Hunan University, Changsha, China, from 1991 to 1997. Since April 2004, he has been a faculty member in the Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai, China. His research interests are numerical methods in electro-magnetic fields, coupled thermo-electromagnetic analysis, microwave filter designs, fiber-optic filter designs, phased arrays, and inverse scattering problems.

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Topic 3: Computational Electromagnetic Methods for Atomic Thin Graphene Characterization

Speaker: Lijun Jiang
University of Hong Kong
ljiang@eee.hku.hk

Abstract of the talk

Graphene, an atomically thin 2-D sheet of carbon atoms in which the atoms are arranged in a honeycomb lattice, has already gained intense attentions from many groups over the world because of its unique electrical, mechanical, and thermal properties. These remarkable properties make it as a promising candidate for semiconductor, tunable nanoantenna, and surface plasmon waveguide, etc. The surface conductivity of graphene is particular of interest to study the electromagnetic properties of graphene such as surface plasmon polarization (SPP). In the absence of external magnetostatic bias, the surface conductivity is a scalar. Otherwise it becomes a tensor.

To quantify the EM properties of graphene, various numerical algorithms have been developed such as MoM, FDTD method, etc. In this talk, we will first discuss the experimental study of Graphene conductivity properties in the microwave region. Then we will discuss the computational electromagnetic methods in solving structures with general graphene sheets. There are two approaches to treat graphene: i) The graphene is considered as a thin layer with finite thickness, thus volumetric meshing is required. With this approach, the surface conductivity is transformed to an equivalent permittivity. ii) The volumetric graphene is modeled as an infinitesimal thin sheet over which a surface-impedance boundary condition (SIBC) is satisfied. Compared with frequency domain methods, time-domain methods have advantages such as broadband characterization with only single simulation, transient response capture, etc. Two specific methods, discontinuous Galerkin's time domain (DGTD) method and PEEC method will be introduced to model and analyze both static and biased graphene structures. The numerical verifications will demonstrate the feasibility and flexibility of the introduced methods. These approaches provide solutions not only graphene characterizations, but also for anisotropic medium analysis in electromagnetic fields.

Lijun Jiang

Dr. Lijun Jiang received the Bachelor Degree in electrical engineering from the Beijing University of Aeronautics and Astronautics in 1993, the Master Degree from the Tsinghua University in 1996, and the Ph.D from the University of Illinois at Urbana-Champaign (UIUC) in 2004. From 1996 to 1999, he was an Application Engineer with the Hewlett-Packard Company (HP). From 2004 to 2009, he has been the Postdoc, the Research Staff Member, and the Senior Engineer at IBM T.J. Watson Research Center. Since Dec. 2009, he has been the Associate Professor at the Department of Electrical and Electronic Engineering, the University of Hong Kong. He was the Senior Visiting Professor at Tsinghua University from Jun. 2013 to Jun. 2014. And he has been the visiting scholar to Professor T. Itoh's group at UCLA since Sept. 2014 and spent his Sabbatical at UCLA during Sept. 2014 to Mar. 2015.

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Topic 4: Silicon Integration and Packaging - the Hardware Pillars of mmWave 5G

Speaker: Dr. Xiaoxiong (Kevin) Gu
IBM T. J. Watson Research Center
xgu@us.ibm.com

Abstract of the talk

Mm Wave technology is rising as a crucial component for 5G radio access and other emerging ancillary wireless networks including Gb/s device-to-device communication and mobile backhaul. This talk covers recent advances in state-of-the-art mm-wave silicon technology, packaging and integrated antenna design in the context of 5G communications. The main challenges in 5G hardware development and the corresponding mitigation strategies are discussed with a focus on RFIC, antenna and packaging integration technologies. The talk emphasizes the following key enablers for the commercial scale deployment of mm-wave technology in the 5G era: 1) highly integrated and complex circuits in silicon technologies, and 2) strategies for IC, package, antenna and board co-design and integration. Through various examples of mmWave transceivers with antennas-in-package demonstrated in hardware, this talk illustrates how these challenges can be addressed for a variety of potential 5G usage scenarios, from PAN to backhaul.

Xiaoxiong (Kevin) Gu

Dr. Xiaoxiong (Kevin) Gu received his Ph.D. in electrical engineering from the University of Washington in 2006. He joined IBM Research as a Research Staff Member in January 2007. His research activities are focused on 5G radio access technologies, optoelectronic and mm-wave packaging, electrical designs, modeling and characterization of communication and computation systems. He has recently worked on antenna-in-package design and integration for mm-wave imaging and communication systems including K-band, V-band and W-band phased-array modules. Dr. Gu has authored and co-authored over 70 technical papers and has 8 issued patents. He received an IBM Outstanding Technical Achievement Award in 2016, four IBM Plateau Invention Awards in 2012 ~ 2016, the IEEE EMC Symposium Best Paper Award in 2013, two SRC Mahboob Khan Outstanding Industry Liaison Awards in 2012 and 2014, the Best Conference Paper Award at IEEE EPEPS in 2011, IEC DesignCon Paper Awards in 2008 and 2010, the Best Interactive Session Paper Award at IEEE DATE in 2008, and the Best Session Paper Award at IEEE ECTC in 2007. Dr. Gu is the co-chair of Professional Interest Community (PIC) on Computer System Designs at IBM. He is a Senior Member of IEEE and has been serving on the technical program committees for numerous IEEE Conferences (IMS, EPEPS, ECTC, EDAPS) and DesignCon.

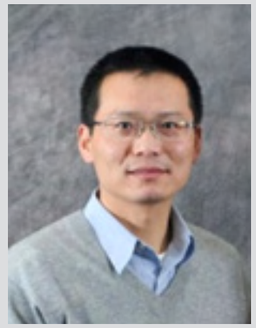
Workshop -III

Analyzing Power Supply Induced Jitter in I/O Buffers: from Simple to Complex
Organizer: Prof. Jun Fan
Missouri University of Science and Technology, USA
jfan@mst.edu

Dec 14(Thu), 2017, 14:30-15:00
201, Lecture Theatre West

Topic 1: Power Supplied Induced Jitter: Concept and Transfer Function

Speaker: Prof. Jun Fan
Missouri University of Science and Technology, USA
jfan@mst.edu



Abstract of the talk

With continuous increase of data rate, power supply induced jitter (PSIJ) becomes an important factor for high-speed signal propagation. This talk introduces the basic concept of PSIJ through the analysis of a simple I/O buffer. A methodology based on the transfer function from the noise voltage generated in power distribution network to output jitter is then discussed. Examples are used to validate the methodology and illustrate its application.

Jun Fan

Jun Fan (S'97-M'00-SM'06-F'16) received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received his Ph.D. degree in Electrical Engineering from the University of Missouri-Rolla in 2000. From 2000 to 2007, he worked for NCR Corporation, San Diego, CA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently a Professor and Director of the Missouri S&T EMC Laboratory. Dr. Fan also serves as the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intra-system EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs. In the IEEE EMC Society, Dr. Fan served as the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, the Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He currently is an associate editor for the IEEE Transactions on Electromagnetic Compatibility and IEEE EMC Magazine. Dr. Fan received an IEEE EMC Society Technical Achievement Award in August 2009.

Dec 14(Thu), 2017, 15:00-15:30
201, Lecture Theatre West

Topic 2: A statistical link analysis method considering ISI, supply voltage fluctuations, and SSO

Speaker: Prof. Jingook Kim
Ulsan National Institute of Science and Technology, Korea
jingook@unist.ac.kr

Abstract of the talk

The previous timing specifications have provided only the total worst case jitter. The design approach checking the setup and hold time violations due to the total worst jitter was sufficient at lower data rates; however, it can lead to significant errors at higher data rates, resulting in over- or under-designed systems. Hence, the statistical link specification methods have been proposed to improve the predictability of maximum attainable data rate. In addition to inter-symbol interference (ISI), switching of numerous logic circuits and I/O buffers inside integrated circuits (ICs) can result in significant voltage drop and ripple in the power distribution network (PDN). Also, the pattern-dependent simultaneous switching outputs (SSO) and resultant output jitter is one of the major performance limiters as data rate scales higher. This talk deals with an enhanced statistical link analysis considering ISI, supply voltage fluctuations, and SSO.

Jingook Kim

Jingook Kim received his B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejon, Korea, in 2000, 2002, and 2006, respectively. From 2006 to 2008, he was with DRAM design team in Memory Division of Samsung Electronics, Hwasung, Korea, as a senior engineer. From January 2009 to July 2011, he worked for the EMC Laboratory at the Missouri University of Science and Technology, Missouri, USA, as a postdoc fellow. In July 2011, he joined the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, where he is currently an associate professor. He has authored or co-authored over 100 journal and conference papers. His current research interests include high-speed I/O circuits design, 3D-IC, EMC, ESD, RF interference.

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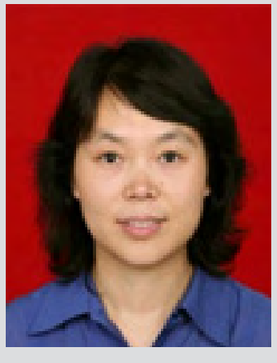
Topic 3: Analytic Calculation of Jitter Induced by Power and Ground Noise Based on IBIS I/V

Speaker: Xiuqin Chu
Xidian University
xqchu@mail.xidian.edu.cn



Abstract of the talk

Supply fluctuation is one of the most significant factor that causes jitter in high-speed I/O links. Traditional SPICE simulation or measuring method for power supply induced jitter (PSIJ) is quite time consuming and draining on resource. IBIS model is a popular standard for electronic behavioral specifications of digital integrated circuit I/O characteristics. This presentation reports a method of analytic jitter transfer functions for supply fluctuations by solving two order differential equations based on IBIS I/V characteristics and pin package parameters. In this method the spectrum of output jitters induced by power supply fluctuations is obtained in frequency domain. Then the time jitter is obtained after transforming the jitter frequency spectrum into time domain. The method is validated by comparing the analytic calculation results with HSPICE simulated results for a DDR4 output buffer.

This method provides the completely analytic solution for noise-to-jitter sensitivity based on IBIS I/V curve and package parameters without any measuring or simulation. It is efficient for all I/O buffers in high-speed links.

Xiuqin Chu

Xiuqin Chu received the B.S. degree in electronic engineering at Xi'an Shiyou University, Xi'an, China, in 1994. She received her M.S. and Ph.D. degrees at Xidian University, Xi'an, China, in 1997 and 2003, respectively.

In April 1997, she joined the Xidian University and is currently an Associate Professor with Electronic and Engineering institute. From March 2016 to April 2017, she was a Visiting Scholar with the EMC Laboratory, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Missouri, USA. Her current research interests include signal/power integrity and jitter analysis in high-speed digital systems.

Workshop -IV

Machine Learning for Hardware Design
Organizer: Madhavan Swaminathan
Georgia Institute of Technology
madhavan@ece.gatech.edu

Dec 14(Thu), 2017, 13:30-14:00
204, Lecture Theatre West

Speaker: Madhavan Swaminathan
Georgia Institute of Technology
madhavan@ece.gatech.edu

Abstract of the talk

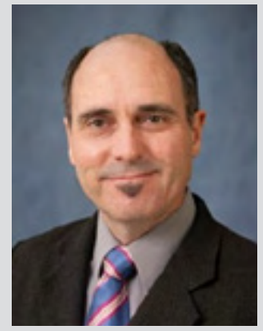
Moore scaling and More than Moore scaling have led to the miniaturization of electronic systems over the last several decades. This trend is expected to continue into the future with applications related to high performance computing, automotive, internet of things and health care being major drivers. EDA tools have allowed the electronics industry to successfully manage more than five decades of exponential increase in design complexity. These tools have always relied on simulation for the development of low-cost, safe, energy-efficient electronic systems ranging from smart phones to airplanes. Though these tools have reduced the number of design re-spins, the observed failures during qualification testing continue to be a direct result of insufficient modeling capability. Therefore, a new and better approach to generating models are necessary that can advance the capabilities of EDA. This special session explores the use of Machine Learning based modeling as a way to design and optimize electronic systems. The speakers in this workshop cover diverse areas related to IC, Package and System integration.

Madhavan Swaminathan

Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE) and Director of the Center for Co-Design of Chip, Package, System (C3PS), Georgia Tech. He formerly held the position of Joseph M. Pettit Professor in Electronics in ECE and Deputy Director of the NSF Microsystems Packaging Research Center, Georgia Tech. Prior to joining Georgia Tech, he was with IBM working on packaging for supercomputers. He is the author of 450+ refereed technical publications, holds 29 patents, primary author and co-editor of 3 books, founder and co-founder of two start-up companies (E-System Design and Jacket Micro Devices) and founder of the IEEE Conference Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the packaging society on Signal Integrity in the Asian Region. He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE EMC society. He received his MS and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively

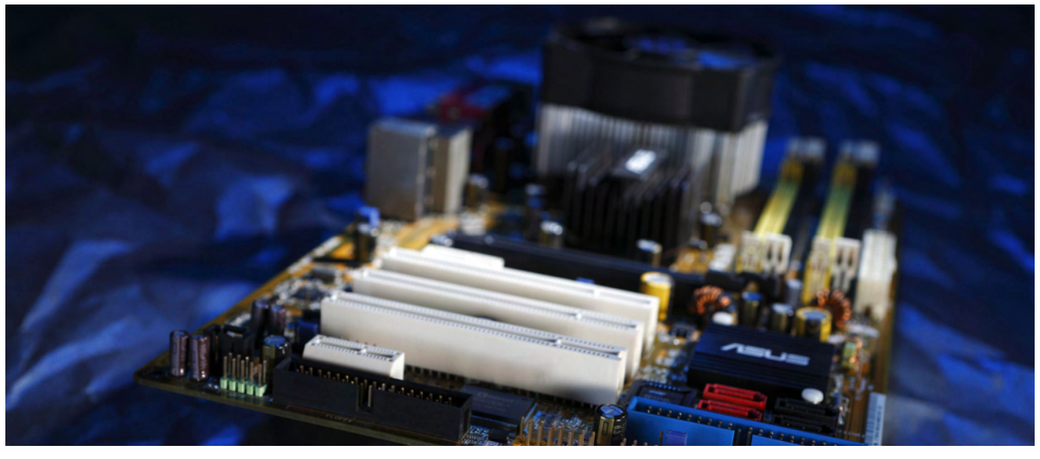
Dec 14(Thu), 2017, 14:00-14:30
204, Lecture Theatre West

Speaker: Prof. Paul Franzon
North Carolina State University
paulf@ncsu.edu



Paul D. Franzon

Paul D. Franzon is currently the Cirrus Logic Distinguished Professor of Electrical and Computer Engineering and Director of Graduate programs in ECE at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom and three companies he cofounded, Communica, LightSpin Technologies and Polymer Braille Inc. His current interests center on the application of, technology and design of complex microsystems incorporating VLSI, advanced packaging and nano-electronics. He has lead several major efforts and published over 300 papers in these areas. In 1993 he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, in 2003, selected as a Distinguished Alumni Professor, received the Alcoa Research Award in 2005, and the Board of Governors Teaching Award in 2014. He served with the Australian Army Reserve for 13 years as an Infantry Soldier and Officer. He is a Fellow of the IEEE.



Oral Sessions

2017-12-15 AM
9:50-11:45
201, Lecture Theatre West

Oral Session: 1
Electronic Design of MM-Wave Integrated Circuits and Systems
Organizer: Kai Kang
Co-Chairs: Yunqiu Wu and Kai Kang

09:50-10:10	Integration of a 60 GHz Packaged LTCC Grid Array Antenna with an Amplifier (invited) Peng-Fei Sun, Tang Liu, Jian Zhang, Lin-Pu Huang
10:10-10:30	A 27.5-43.5 GHz High Linearity Up-Conversion CMOS Mixer for 5G Communication Zhilin Chen, Zhiqing Liu, Zhengdong Jiang, Pengxue Liu, Huihua Liu, Yunqiu Wu, Chenxi Zhao, Kai Kang
10:30-10:45	DC-110GHz Continuous Variable Attenuator Based on 65nm CMOS Process Jiamei Lv, Jincai Wen, Long Wang, Qingping Zhang, Yonghe Wang
10:45-11:00	A Wide-Range, High-Resolution Time to Digital Converter Using a Three-Level Structure Mei Jiang, Yanzhe He
11:00-11:15	A Package-Level Driver Amplifier with 134% Relative Bandwidth Dong Chen, Zhao Xing, Zhilin Chen, Chenxi Zhao, Huihua Liu, Kai Kang
11:15-11:30	Graphene Based Thermoelectric Energy Harvesting in 3D ICs Shi-Yun Zhou, Cheng Zhuo, Qiu Min, Er-Ping Li
11:30-11:45	Multi-GHz Microstrip Transmission Lines Realised by Screen Printing on Flexible Substrates Yizhi Shi, Zhenzhen Jiang, Sang Lam, Mark Leach, Jingchen Wang, Eng Gee Lim

2017-12-15 AM
9:50-12:00
204, Lecture Theatre West

Oral Session: 2
High-Performance Interconnects and Microwave Circuits
Organizers: Xiaochun Li and Min Tang
Co-Chairs: Xiaochun Li and Min Tang

09:50-10:10	Simple and Fast Method of On-Board Decoupling Capacitor Selection and Placement (invited) Guobing Han
10:10-10:30	A Novel EBG Microstrip Line with Noise Suppression (invited) Xiang-Ting Wang, Xiao-Chun Li, Jun-Fa Mao
10:30-10:45	Substrate Integrated Waveguide Cavity Backed Mushroom Antenna with Broadband and High Gain Hui-Fen Huang, Sun Shuai
10:45-11:00	Electrothermal Co-Simulation of a Two-Chip Power Delivery Network in Frequency Domain Na Li, Junfa Mao, Wen-Sheng Zhao, Min Tang, Wen-Yan Yin
11:00-11:15	Investigation of the Capacitance Compensation Structure for Wire-Bonding Interconnection in Multi-Chips Module Haoran Zhu, Yu-Fa Sun, Xianliang Wu
11:15-11:30	Numerical Calibration on Complex Propagation Constants of Grounded Coplanar Waveguides Liang Chen, Min Tang, Junfa Mao, Haikun Yue, Yang Tang
11:30-11:45	Study of the Electro-Thermal Collaborative Cooling Based on Energy Harvesting for Thermoelectric Coolers Ning Wang, Zhiyuan Liu, Hongzhi Jia
11:45-12:00	Simulation of Graphene Nanoribbon Interconnects by Boltzmann-Poisson Approach under Relaxation Time Approximation Min Tang, Junfa Mao

2017-12-15 AM
9:50-12:00
207, Lecture Theatre West

Oral Session: 3
Multiphysics Modeling of Devices for Low Power ICs
Organizers: Wenchao Chen and Jun Huang
Co-Chairs: Wenchao Chen and Yang Xu

09:50-10:10	High Performance Graphene-Silicon UV and IR Photodetectors (invited) Yang Xu
10:10-10:30	Multiphysics Modeling and Simulation of Ultra-Thin Channel Germanium on Insulator (GeOI) MOSFETs (invited) Wenchao Chen, Manxi Wang, Wen-Yan Yin, Er-Ping Li
10:30-10:45	Hole Mobility Model for Si Double-Gate Junctionless Transistors (invited) Fan Chen, Jun Z. Huang, Kang-Liang Wei
10:45-11:00	The Performance Improvement in SiGeSn/GeSn P-channel Hetero Line Tunneling FET (HL-TFET) Hongjuan Wang, Genquan Han, Xiangwei Jiang Zhang, and Yue Hao
11:00-11:15	Extraction of Model Card in Metal Oxide Thin-Film Transistor by Fitting Measured Curves with RPI Model and Simulation of Circuits Xixiong Wei, Feng Zhuang, Zheng Zhou, Weijing Wu, Xiaoyu Ma, Wanling Deng
11:15-11:30	Optimization Model for Flexible Piezoelectric Film in Self-Powered Pressure Sensor Jiatong Huang, Yiping Zhu Pingxiong Yanga, Lianwei Wanga, and Paul K. Chu
11:30-11:45	Using Low Noise Induction Magnetometer for Online Monitoring of the Induction Machine Yong Liu, Kai Liu, Wenbing Li, Huan Zheng
11:45-12:00	Modeling and Simulation of Si/PEDOT:PSS Planar Heterojunction Photovoltaics by Finite Element Method Wenchao Chen, Manxi Wang, Xiaofan Yang, Wen-Yan Yin, Er-Ping Li

2017-12-15 PM
13:30-17:40
201, Lecture Theatre West

Oral Session: 4
Carbon-based Interconnects for 3-D Integrated Systems
Organizers: Libo Qian and Wen-Sheng Zhao
Co-Chairs: Libo Qian and Qingfeng Zhang

13:30-13:50	Electrical Modeling and Analysis of Carbon Based Three Dimensional Integration (invited) Libo Qian, Jifei Sang, Yidie Ye, Ge Shi
13:50-14:10	Closed-Form Internal Impedance Model of Mixed Carbon Nanotube Bundles for 3-D ICs Qijun Lu, Zhangming Zhu, Yintang Yang, Xiangkun Yin, Xiaoxian Liu, Chenbing Qu, Yang Liu
14:10-14:25	Modeling of Power Distribution Network Based on Multi-Walled Carbon Nanotube TSVs for 3-D ICs Jing Jin, Wen-Sheng Zhao, Da-Wei Wang, Wen-Yan Yin
14:25-14:40	Electrical Modeling and Analysis of Air-Cavity Through-Silicon Vias (TSVs) Xiaoxian Liu, Zhangming Zhu, Yintang Yang, Qijun Lu, Xiangkun Yin, Yang Liu
14:40-14:55	Double-T Type Equivalent Circuit Modelling Method for TSVs Up To 50GHz Xiangkun Yin, Zhangming Zhu, Yintang Yang, Qijun Lu, Xiaoxian Liu, Yang Liu
14:55-15:10	Electrical Characteristics of GS-TSV in Slow Wave Mode Fengjuan Wang, Gang Wang, Ningmei Yu
15:10-15:25	The Influence of Anti-Pad Array on the Inductance of PCB Power Net Area Fill Qixuan Sun, Siqi Bai, James L. Drewniak, Er-Ping Li

15:25-15:45 Coffee Break

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15:25-15:45 Coffee Break

15:45-16:05 Performance Comparison and Analysis by Electrical Measurement for Through-Silicon Vias (TSV) in Wafer Level Package (invited)
Yu-Chang Hsieh, Chung-Hao Chen, Pao-Nan Lee, Chen-Chao Wang

16:05-16:25 Modeling and Characterization of Polymer-Embedded Through-Silicon Vias (TSVs) in 3-D Integrated Circuits
Chenbing Qu, Zhangming Zhu, Yintang Yang, Ruixue Ding, Xiaoxian Liu, Qijun Lu, Xiangkun Yin

16:25-16:40 Electrical-Thermal Co-Analysis of Through Silicon Via with Equivalent Circuit Model
Qiu Min, Er-Ping Li, Cheng Zhuo, Yong-Sheng Li, Shi-Yun Zhou, Jian-Ming Jin

16:40-16:55 Radiation Emission for Parallel Planes with Vias in Packaging
Panpan Zuo, Wenyuan Cao, Yan Li, Yan-Bo Xu, Hongxing Zheng, Er-Ping Li

16:55-17:10 A Generating Method of Wideband Signal of Array Antennas
Chun Wang, Long Xiao, Chao Ni

17:10-17:25 Atomic Diffusion of Zn in Sn-Zn Based Solder Joints Subjected to High Temperature Aging
Jian-Chun Liu, Long Xiao, Zhi-Jun Yue, Gong Zhang

17:25-17:40 Stochastic LIM for Uncertainty Characterization of Fiber-weave Effect on Coupled Transmission Lines
Xu Chen, Jose E. Schutt-Aine, Andreas C. Cangellaris

Poster Session

2017-12-15 PM
13:30-15:30
Corridor

POSTER SESSION

Co-Chairs: Lin-Sheng Wu and Zhixiang Huang

P. 1 Enhancement of Power Quality in Wind Connected Power Plant Using Static Synchronous Compensator
Sant Ranjan

P. 2 Phase Switched Screen based on Artificial Magnetic Conductors
Yumei Chang, Lijie Xu, Bo Li, Yiming Tang

P. 3 The Application of Wavelet Filtering in the Dynamic Loading Identification System of Rock Roadheaders
Wei Wang

P. 4 Stability Analysis of Coupled Copper-Carbon Nanotube (Cu-CNT) Composite Interconnects
Qiu-Yi Yang, Zi-Han Cheng, Wen-Sheng Zhao, Gao-Feng Wang

P. 5 Modeling of Crosstalk Effects in Carbon Nanotube Based Differential Through-Silicon Via Array
Jin-Wei Pan, Kai Fu, Zi-Han Cheng, Wen-Sheng Zhao, and Gaofeng Wang

P. 6 Analytical Model for 3D IC Temperature Considering Lateral Heat Conduction
Fengjuan Wang, Ningmei Yu

P. 7 Dual Polarization Millimeter-Wave Antenna for Microcell Base Station
Luo Wei, Huang Hui, Wang Bin

P. 8 Research on Model Based Reliability System Engineering Methodology of System in Package
Yutai Su, Guicui Fu, Ye Wang, Hongyan Leng, Hantian Gu

P. 9 Research on the Propagation Properties of EM Wave in Inhomogeneous Plasma Sheath Using DGTD method
Linqian Li, Bing Wei, Qian Yang, Debiao Ge

P. 10 A Compact Ku-Band 6-bit Attenuator in 0.35um SiGe BiCMOS Technology
Wenbo Shi, Kaixue Ma, Shouxian Mou, Fanyi Meng

Oral Sessions

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15:45-17:40
204, Lecture Theatre West

Oral Session: 5
MMIC Design and Packaging
Organizers: Kaixue Ma and Fanyi Meng
Co-Chairs: Kaixue Ma and Fanyi Meng

15:45-16:05 Design of LTCC Package for DGS LPF Switch (invited)
Alit Apriyana, Y. P. Zhang

16:05-16:25 Shielding Can Design for a DDR4 Connector System to Reduce RFI (invited)
Taeho Choi, Soyoung Kim

16:25-16:40 Design of Ku-Band SiGe-HBT Power Amplifier with Through-Silicon-Via Applying 3-D EM Simulation
Guoxiao Cheng, Zhiqun Li, Lei Luo, Yan Yao, Xiaodong He, Boyong He

16:40-16:55 Design of a Low Phase-Noise Oscillator Using Cavity Resonator in Substrate Integrated Suspended Line Technology
Meng Li, Kaixue Ma

16:55-17:10 A High-Isolation Ku-Band SPDT Switch in 0.35μm SiGe BiCMOS Technology
Zhe Fan, Kaixue Ma, Shouxian Mou, Fanyi Meng

17:10-17:25 A Ku-Band 6-Bit Phase Shifter in 0.35-μm SiGe BiCMOS Technology
Xuesong Han, Kaixue Ma, Shouxian Mou, Fanyi Meng

17:25-17:40 A New Band-stop Filter Design with Triple Electric Paths for Passband Extension
Wei Xu, Kaixue Ma, Fanyi Meng, Shouxian Mou

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13:30-17:40
207, Lecture Theatre West

Oral Session: 6
Multiphysics Modeling of Passives and Actives
Organizer: Liang Zhou
Co-Chairs: Liang Zhou and Shaoqiu Xiao

13:30-13:50 Evaluation of Thick Monopole in Rectangular Cavity: An Analytic Approach (invited)
Qi Wu

13:50-14:10 Influence of Loss Mechanisms on High Q Whispering Gallery Mode (WGM) Resonators Suitable for RF Applications (invited)
Victor Silva Cortes, Jonathan Binder, Georg Fischer, Amelie Hagelauer

14:10-14:25 Trapping and Gate Leakage Currents Effects in Large Signal Modeling of Microwave GaN HEMTs (invited)
Shuman Mao, Yuehang Xu, Xiaodong Zhao, Ruimin Xu, Yongbo Chen, Nengwu Gao

14:25-14:40 Comparisons of Power to Failure for Low-Noise Amplifiers under High-Power Microwave Pulses
Xiang Chen, Liang Zhou, Junfa Mao, Wenyan Yin

14:40-14:55 AI Machine Learning Dynamic for 3D-IC Thermal Management for 3-D ICs Using Microchannel Cooling Methods
Yong-Sheng Li, Er-Ping Li

14:55-15:10 Thermal Fatigue Life Analysis of Defective Solder Joints Based on Engelmaier Fatigue Model
JianWei Zuo, Guicui Fu, Yutai Su, Maogong Jiang

15:10-15:25 Novel Application of Ring-Oscillator-Based Sensor for 3D IC Temperature and IR Drop Monitoring
Jin-Chern Chiou, Tzu-Sen Yang, Shang-Wei Tsai

15:25-15:45 Coffee Break

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15:25-15:45 Coffee Break

15:45-16:05 Distributed Matching Network Design for Broadband Power Amplifiers (invited)
Yuan Zhuang, Zhouxiang Fei, Anqi Chen, Yi Huang, Jiafeng Zhou

16:05-16:25 Reconstruction of Sparse Radiation Sources above a Finite Ground Plane (invited)
Chaofeng Li, Huapeng Zhao, Zhizhang Chen, Jun Hu

16:25-16:40 Comparison of Thermal Stress under TCT Between SiC and Si Power Devices Using Direct Chip-Bonding with Ag Sintered Layer on Cu Plate
Masaki Kanemoto, Masaaki Aoki, Akihiro Mochizuki, Yoshio Murakami, Mutsuharu Tsunoda, Goro Yoshinari, Nobuhiko Nakano

16:40-16:55 Investigation of Graphite for Radiation Mitigation and Thermal Management in Heat Sink
Ping Cheng, Le Zhang, Qiu Min, Bin Li, Yaojiang Zhang, Er-Ping Li

16:55-17:10 Study on the Touch Risk of High Density Packaging Bonding Wire under Mechanical Shock Condition
Hantian Gu, Ming Zhu, Wei Zhang, Hengjing Zhu, Lei Zhang

17:10-17:25 A High Resolution Time Amplifier Based Time-to-Digital Converter for 3D Image Sensor
Xiangliang Jin, Can Cao

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201, Lecture Theatre West

Oral Session: 7
Advanced Packaging and 3D Integration
Organizer: Cheng Zhuo
Co-Chair: Cheng Zhuo and Wenjian Yu

08:00-08:20 Embedded Ceramic Interconnect Bridge in Organic Substrate for Heterogeneous Integration and Multi-Chip Packaging (invited)
Boping Wu

08:20-08:40 Application of Hybrid PCB Stackup (invited)
Yinglei Ren, Maoxin Yin, Chunfei Ye, Xiaoning Ye

08:40-08:55 Die-to-Package Coupling Extraction for Fan-Out Wafer-Level-Packaging
Yarui Peng, Dusan Petranovic, Sung Kyu Lim

08:55-09:10 Investigation of Electrical Discontinuity in Flip-chip Package
Yan-Bo Xu, Xiaoli Yang, Yan Li, Panpan Zuo, Hongxing Zheng, Er-Ping Li

09:10-09:25 Design and Electrical Performance Analysis on Coreless Flip Chip BGA Substrate
Chih-Yi Huang, Chen-Chao Wang, Tsun-Lung Hsieh, Cheng-Yu Tsai

09:25-09:40 Design of 3-Dimensional Wafer Level Integrations of Slow-Wave Coupled Oscillators
Yu-Jie Hua, Chengrui Zhang, Liang Zhou, Junfa Mao

09:40-09:55 Dog-Bone Geometry Modeling Based on PEEC for Package PDN
Tuomin Tao, Hanzhi Ma, Chenxi Huang, Ying S. Cao, James Drewniak, Er-Ping Li

9:55-10:15 Coffee Break

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15:25-15:45 Coffee Break

10:15-10:35 Efficient Capacitance Modeling and Extraction for the Cylindrical Inter-Tier-Vias in 3-D IC
Wenjian Yu

10:35-10:55 Power Integrity Challenges of Modern SoCs and ASICs
Zhongyang Liu, Houle Gan

10:55-11:10 Novel LC Resonant Clocking for 3D IC Using TSV- Inductor and Capacitor
Shaoheng Luo, Baixin Chen, Ke Li, Cheng Zhuo, Yiyu Shi

11:10-11:25 Signal and Power Integrity (SI/PI) Analysis of Heterogeneous Integration Using Embedded Multi-Die Interconnect Bridge (EMIB) Technology for High Bandwidth Memory (HBM)
Kyungjun Cho, Youngwoo Kim, Hyunsuk Lee, Gapyeol Park, Subin Kim, Kyungjune Son, Sumin Choi, Joungho Kim

11:25-11:40 The Harmonics Impact Study of a DC-DC Buck Converter Through a Power Delivery Network
Vijender Kumar Sharma, Jai Narayan Tripathi, Hitesh Shrimali, Rakesh Malik

11:40-11:55 On-Chip Layout Optimization of Synchronous DC-DC Buck Converter for EMI Reduction
Soyeon Joo, Jisoo Hwang, Eunseok Song and SoYoung Kim

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8:00-11:55
204, Lecture Theatre West

Oral Session: 8
High-Performance Miniaturized Passives for SoP
Organizers: Lin-Sheng Wu and Xiu-Yin Zhang
Co-Chairs: Lin-Sheng Wu, Yongle Wu and Xiu-Yin Zhang

08:00-08:20 High Performance Balanced-to-Unbalanced Filtering Power Divider (invited)
Wenjie Feng, Rui Yin, Wenquan Che

08:20-08:40 Compact LTCC Filtering Switch with High Isolation Based on Coupling Control
Xiu Yin Zhang, Jin-Xu Xu

08:40-08:55 An Approach to 1-to-3 Way Microstrip Balanced-to-Balanced Power Divider/Combiner
Bin Xia, Lin-Sheng Wu, Jun-fa mao

08:55-09:10 Filtering Balanced-to-Single-Ended Power Divider with Arbitrary Power Division Ratio
Jin Shi, Kai Xu

09:10-09:25 Differential Dual-Band Filter With Flexible Frequency Ratio Using H-Shaped Composite Resonator for SCDMA and LTE Applications
Pin Wen, Zhewang Ma, Haiwen Liu, Baoping Ren, Xuehui Guan

09:25-09:40 Miniaturized Substrate Integrated Waveguide Filtering Crossover
YaLi Zhou, Kang Zhou, Jindong Zhang, Chunxia Zhou, Wen Wu

09:40-09:55 A Novel Design of Miniature Filter-Antenna with Broad Stop-Band Characteristic
Liang Chen, Ben Ma, Weijun Wu, Qifeng Liu

9:55-10:15 Coffee Break

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9:55-10:15 Coffee Break

10:15-10:35 Unidirectional Reciprocal DC-block Impedance Transformer with Flatness and Broadband Negative Group Delay Characteristics (invited)
Y. Wu, H. Wang, Z. Zhuang, Y. Liu

10:35-10:55 A Low Profile Filtering Antenna Based on Metasurface
Peng Fei Hu, Yongmei Pan

10:55-11:10 Wideband Filters on High-Resistivity Silicon Substrate for 5G High-Frequency Applications
Lin-Sheng Wu, Jun-fa Mao, Fang Hou, Jian Zhu

11:10-11:25 Compact Bandpass Filter Based on Hybrid Spoof Surface Plasmon and Substrate Integrated Waveguide Transmission Line
Karthik Rudramuni, Krishnamoorthy Kandasamy, Abhishek Kandwal, Qingfeng Zhang

11:25-11:40 Substrate Integrated Waveguide Dual-Mode Dual-Band Filter with Multilayered Configuration
Kang Zhou, Chunxia Zhou, Wen Wu

11:40-11:55 The Environment Electromagnetic Noise Eliminating Method Base on Self-Adaptive Filter
Nan Wu, Maosong Wu, Fengtao Wu, Jianbin Li

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8:00-11:40
207, Lecture Theatre West

Oral Session: 9
Antenna and Packaging Systems
Organizers: Hongli Peng and Yaoping Zhang
Co-Chairs: Hongli Peng and Yaoping Zhang

08:00-08:20 The Strong Scattering Effect of Transcranial Vortex Microwave Beam and Its Application in Intracranial Hemorrhage High Quality Imaging
Dang-Dang Wang, Hong-Li Peng, Bin-Xian Gu

08:20-08:40 Intracranial Focusing and Strong Scattering Effects of Transcranial Vortex Microwave Beam
Can Li, Dang-Dang Wang, Hong-Li Peng, Bin-xian Gu

08:40-08:55 A New Fabry-Perot Resonance Antenna Based on Graphene
Yan Cheng, Lin-Sheng Wu, Yao-Ping Zhang

08:55-09:10 Stacked Patch Array in LTCC for 28 GHz Antenna-in-Package Applications
Ge Guo, Lin-Sheng Wu, Yao-Ping Zhang, Jun-Fa Mao

09:10-09:25 Physically Derived Micro-Modeling Circuit for Loop Antenna of Arbitrary Shape
Yuhang Dou, Ke-Li Wu

09:25-09:40 A Design of Wide-Band Stacked Patch Antenna with Extracted Coupling Matrix
Yu-Xuan Wei, Min Tang, Sheng-Jie Guo, Lin-Sheng Wu, Yao-Ping Zhang, Junfa Mao

09:40-09:55 Dual-Circular-Polarization Vivaldi Antenna with Broad Beamwidth and Wide Bandwidth
Jiawei Ma, Chang Meng, Puyu Liu, Zhenhong Fan, Rushan Chen

9:55-10:15 Coffee Break

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10:15-10:35 A New Compact Dual-Polarized Co-Axial Full-Band Antenna for 2G/3G/LTE Base Station Applications
Wei Wu, Hongli Peng, Junfa Mao

10:35-10:55 A New Hilbert Structure Based Meta-Surface for Improving Isolation Between Two Antenna Elements
Gong-Jin Li, Hua-Shan Luan, Hong-Li Peng, Jin Wang

10:55-11:10 The Radiation Characterization Analysis of Dielectric Antenna Based on S-PEEC Model
Yang Jiang, Yuhang Dou, Ke-Li Wu

11:10-11:25 Zipper Antennas for the Applications of Body-Centric Networks
Chenglong Lin, Gaosheng Li, Xianjun Huang, Yanfei Dong

11:25-11:40 Mapping the Foam-induced Dielectric Anisotropy for High-Speed Cables
Qiwei Zhan, Rui Zhang, James Baker, Henning Hansen, Qing-Huo Liu

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13:30-17:25
201, Lecture Theatre West

Oral Session: 10
FDTD / FDFD for Multiphysics Simulation of Mulitscale Structures
Organizers: Wei E.I. Sha and Zhixiang Huang
Co-Chairs: Wei E.I. Sha and Zhixiang Huang

13:30-13:50 Modeling Hybrid EM-Circuit System with Wave Equation-Based Discontinuous Galerkin Time Domain Method (invited)
Cheng-Yi Tian, Peng Wang, Yan Shi

13:50-14:10 EMI Analysis of Field-Line-Circuit Coupling Model Based on Time Domain Integral Equation Method
Shitao Chen, Tiancheng Zhang, Dazhi Ding, Rushan Chen

14:10-14:25 An Optimized Artificially Anisotropic WCS-FDTD Method with Reduced Numerical Dispersion
Kaikun Niu, Zhixiang Huang, Minquan Li, Xianliang Wu

14:25-14:40 Simulation of Radiative Cooling with FETD method
Huan Huan Zhang, Wei E. I. Sha, Zhixiang Huang, Yu Zhang

14:40-14:55 The Techniques to Accelerate Solving Electromagnetic Scattering Over Wide Angles Based on Prior Knowledge of Excitations
Xinyuan Cao, Mingsheng Chen, Xianliang Wu, Meng Kong, Liang Zhang, Qi Qi

14:55-15:10 Efficient Calculation of Near-Field from PDN Using Equivalent Magnetic Current Modal
Wenyuan Cao, Yan Li, Panpan Zuo, Er-Ping Li

15:10-15:25 The Efficient Equivalent Model for Decoupling Capacitors of Power Distribution Network
Sichen Yang, Er-Ping Li, Ying S. Cao, Hanzhi Ma, Jonghyun Cho, Albert Ruehli, James Drewniak

15:25-15:45 Coffee Break

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15:25-15:45 Coffee Break

15:45-16:05 Band Structure of Plasmonic Crystals with an Eigenvalue Algorithm
Hui Wang, Wei E. I. Sha, Zhixiang Huang, Xianliang Wu

16:05-16:25 Selection of UPML Parameters in DGTD Calculation
Qian Yang, Bing Wei, Linqian Li, Debiao Ge

16:25-16:40 Modeling the Effects of Transmission Media on Power Supply Induced Jitter
Jai Narayan Tripathi, Ramachandra Achar

16:40-16:55 Analysis of Radio Frequency Interference Due to High Speed Digital Signals
Jihoon Kim, Jisoo Hwang, Eunseok Song, Soyoung Kim

16:55-17:10 Plane-Pair PEEC Method for Impedance Analysis of Multi-Slots Power Distribution Network with Experimental Validation
Yan Li, Zhi-Yi Gao, Wenyuan Cao, Panpan Zuo, Yan-Bo Xu, Xiaoli Yang, Cheng Ping, Yong-Sheng Li, Le Zhang, Hongxing Zheng, Er-Ping Li

17:10-17:25 An Efficient Approximation Method for Delay-Rational Model of Multiconductor Transmission Line
Xin Chen, Qiang Tang, Mei Song Tong

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13:30-17:25
204, Lecture Theatre West

Oral Session: 11
CEM for Advanced Integration and Packaging Systems
Organizers: Xiaomin Pan and Dazhi Ding
Co-Chairs: Xiaomin Pan and Dazhi Ding

13:30-13:50 The Self-Consistent Model Incorporating the Gain into a Dispersive Metamaterial Nanostructure (invited)
Zhixiang Huang, Yongkang Zhang, Ming Fang, Kaikun Niu, Xingang Ren, Xianliang Wu

13:50-14:10 Electromagnetic Modeling of Shielding Enclosure for Chip Structures (invited)
Qing Xu, Meisong Tong

14:10-14:25 Numerical Modeling of PCB Power/Ground Plate-Pairs by DGTD Method Taking into Account Decoupling Capacitors
Ping Li, Lijun Jiang, Hakan Bagci

14:25-14:40 Study on a Poisson's Equation Solver Based on Deep Learning Technique
Wei Tang, Tao Shan, Xunwang Dang, Maokun Li, Fan Yang, Shenheng Xu, Ji Wu

14:40-14:55 Co-Simulation and Co-Optimization Strategy for Active Absorber with Periodic Structure
Jinchao Mou, Zhongxiang Shen

14:55-15:10 Analytical Solutions of Temperature Distributions Based on Fourier Series for Wafer Level Heterogeneous Integrations
Wen-Wu Ruan, Chengrui Zhang, Liang Zhou, Junfa Mao

15:10-15:25 Electromagnetic-Circuit Cosimulation Based on Hybrid Explicit-Implicit DGTD and SBF Macromodel
Ping Yuan, Huan Zhang, Li Jiang, Daniel Garcia Donoro, Yu Zhang

15:25-15:45 Coffee Break

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15:25-15:45 Coffee Break

15:45-16:05	Simulating Exciton Delocalization in Organic Solar Cells by a Modified Drift-Diffusion Model Zi Shuai Wang, Wallace C.H. Choy, Wei E. I. Sha
16:05-16:25	Fast Calculation of Electric Field via Impedance Matrix of Volume-Surface Integral Equation Yan-Nan Liu, Xiao-Min Pan, Xin-Qing Sheng
16:25-16:40	Electromagnetic Simulations of a Neuromorphic Hardware Using PEEC and Memristor SPICE Models Wooryong Lee, Junsik Park, Jingook Kim
16:40-16:55	Machine Learning for Complex EMI Prediction, Optimization and Localization Hang Jin, Le Zhang, Han-Zhi Ma, Si-Chen Yang, Xiao-Li Yang, Er-Ping Li
16:55-17:10	Broadband Diffuse Scattering Metasurface with Units of Randomly Distributed Sizes Lina Qiu, Gaobiao Xiao, Xianghong Kong
17:10-17:25	A Review of Zero Index Metamaterial Jianyu Lin, Dongying Li, Wenxian Yu

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13:30-17:40
207, Lecture Theatre West

Oral Session: 12
Emerging Materials and Device Technologies for ICs and Systems
Organizer: Yuehang Xu
Co-Chairs: Chenxi Zhao and Yang Xu

13:30-13:50	Heterogenous Integration of III-V MMIC and Si CMOS (invited) Lishu Wu, Yuechan Kong, Wei Cheng, Youtao Zhang, Tangsheng Chen
13:50-14:10	An Ultra-Low Power (ULP) Zero-Current-Detector (ZCD) Circuit for Switching Inductor Converter Applied in Energy Harvesting System (invited) Shiquan Fan, Zhongming Xue, Zhuoqi Guo, Wei Gou, Xu Yang, Li Geng
14:10-14:25	Circuit Interpretation and Perturbative Analysis of Differential-to-Common Mode Conversion due to Bend Discontinuities (invited) Xinglong Wu, Flavia Grassi, Sergio A. Pignari, Paolo Manfredi, Dries Vande Ginste
14:25-14:40	Key Technologies of Solid State Devices on Terahertz Yong Zhang, Tianhao Ren, Wei Zhao, Shuang Liu, Oupeng Li
14:40-14:55	Physical-Based Simulation of DC Characteristics of Hydrogen-Terminated Diamond MESFETs Yu Fu, Yuehang Xu, Ruimin Xu, Jianjun Zhou, Yuechan Kong
14:55-15:10	48-to-5/12 V Dual Output DC/DC Converter for High Efficiency and Small Form Factor in Electric Bike Applications Dong Yun Jung, Hyun Gyu Jang, Minki Kim, Junbo Park, Hyun Soo Lee, Chi Hoon Jun, Sang Choon Ko, Seok-Ho Son, Jong Moon Park
15:10-15:25	Development of Advanced AlGaN/GaN HEMTs Large Signal Model Yuehang Xu, Shuman Mao

15:25-15:45 Coffee Break

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207, Lecture Theatre West

15:25-15:45 Coffee Break

15:45-16:05 CMOS 90 nm Multi-Bias Transistor Model Up to 66 GHz (invited)
Yunqiu Wu, Shili Cong, Chenxi Zhao, Huihua Liu, Kai Kang

16:05-16:25 A Novel Interconnect Material for the Challenges in High Speed and High Reliability Chips (invited)
Cher Ming Tan

16:25-16:40 Integration and Packaging 2D Electronics and Nanosystem
Philip Feng

16:40-16:55 Design and Analysis of an Efficient High Holding Voltage SCR for ESD Protection
Zi-Jie Zhou, Xiangliang Jin

16:55-17:10 An Electrothermal Large Signal Model of GaN HEMTs Foundry Process
Changsi Wang, Yongbo Chen

17:10-17:25 Active Balancing Charging Module with Continuous and Controllable Isolation for Battery Management System
Jian Ouyang, Ping Zhang, Shiyong Wang, Huiqi Li

17:25-17:40 An Identification Method of Counterfeit Components Based on Physical Analysis Test Technology
Zhengping Chen, Sujuan Zhang, Yao Qiu

State Key Laboratory of Complex Electromagnetic Environment Effects on Electronics and Information System

电子信息系统复杂电磁环境效应国家重点实验室

State Key Laboratory of Complex Electromagnetic Environment Effects on Electronics and Information System (CEMEE SKL) was established in October 2012 under the approval of Ministry of Science and Technology (MOST) of China. The laboratory aggregates the domestic dominant research communities, focuses on fundamental and advanced issues of complex electromagnetic environment effects on electronics and information system, and develops the researches on effects mechanisms and application fundamentals. The laboratory addresses itself to construct a world-leading comprehensive scientific research platform, as well, to facilitate the development of scientific innovations and key technical abilities of our high-performance electronics and information system.

The laboratory has many leading scientists such as 973 chief technical experts, outstanding young persons and 863 experts. In recent years, the laboratory has undertaken more than 40 national high-tech development projects and national key projects of basic safety researches, and won the Second Class Prize of the State Science and Technological Progress Award once, together with the ministerial level scientific and technological progress award several times. Until now, the laboratory has over 40 authorized or accepted national invention/defense patents. 12 monographs and more than 300 papers are published, in which over one hundred are SCI/EI indexed.

Aiming at the development needs of electronics and information system, the laboratory reinforces the innovative teams' construction and talent cultivation; focusing on the fundamental and advanced problems of complex electromagnetic environment effects, the laboratory carries out the exploratory and innovative researches. Both domestic and international cooperation and academic exchange are preferred. The laboratory is conducted to effectively enhance the adaptability of electronics and information system for complex electromagnetic environment, to provide critical theoretical approaches and technical support for systemic argument, design, development, test and application, to solve the bottleneck issues within the progress of electronic and information system in society development, public safety and national defense constructions, to advance the development of basic theory of complex electromagnetic environment effects on electronics and information system, as well as to promote the development of electronics and information system.

电子信息系统复杂电磁环境效应国家重点实验室（CEMEE 国家重点实验室）于 2012 年 10 月获国家科技部批准成立。实验室汇聚国内优势研究力量，紧密围绕电子信息系统复杂电磁环境效应的基础性、前沿性课题，开展效应机理和应用基础的研究，努力打造具有国际领先水平的综合性科研平台，促进高性能电子信息系统领域科技创新和关键技术攻关能力提升。

实验室拥有多名 973 技术首席、杰青、863 专家等高层次领域人才。近年来，先后承担国家高技术发展计划项目、国家安全重大基础研究项目 40 余项，获国家科技进步二等奖 1 项，部委级科技进步奖多项，授权和受理国家发明（国防）专利 40 余项，出版专著 12 部，发表论文 300 余篇，其中 SCI、EI 检索 100 余篇。

实验室将针对电子信息系统发展需求，加强创新团队建设和人才培养工作，围绕复杂电磁环境效应领域基础理论与前沿科学问题开展探索性、创新性的研究，同时积极开展国内外技术合作与学术交流，以期有效增强电子信息系统对复杂电磁环境的适应性，为其系统论证、设计、研制、试验、应用提供重要的理论方法与技术支撑，解决社会发展、公共安全、国防建设中电子信息技术发展的瓶颈问题，推动电子信息系统复杂电磁环境效应基础理论的发展，提升电子信息系统的发展水平。

Science and Technology on Electromagnetic Compatibility Laboratory

电磁兼容性重点实验室

State key laboratory of electromagnetic compatibility (EMC) was founded in 1996, which is the only national level laboratory of EMC in China. The policy of the lab is "Opening-Flowing-Combining-Competing". The lab is an excellent platform, in which scientific exploration, innovation and basic research are being put in practice. The lab has won the titles of "National Advanced Collective of Professional and Technical Personnel" and "National Technology Innovation Team". Lots of outstanding scientific research personnel are cultivated in the lab.The main research directions of the lab are listed in follow.

· Electromagnetic Environment Characteristics and Electromagnetic Radiation Hazards Protection

· Electromagnetic Compatibility Prediction, Design and Optimization

· Electromagnetic Compatibility Experiment Technology

Through a series of technology improvement projects, the lab has built the advanced experimental facility group, and possessed systematic and powerful EMC test ability. The EMC experimental facility of the lab are comprehensive, including large anechoic chamber, reverberation chamber, GTEM, antenna test field, electromagnetic emission test equipment, electromagnetic susceptibility test equipment and etc. The objective of the lab is to become domestic first-class EMC research base and academic center. We will strive to build a first-class EMC public research platform, gather a group of first-class EMC scientific research personnel, and create first-class EMC technology achievements.

电磁兼容性重点实验室 1993 年经国防科工委批准筹建，1996 年 4 月 22 日正式运行，是我国电磁兼容领域唯一的国家级重点实验室。实验室曾先后获“全国专业技术人才先进集体”和 “国防科技创新团队”称号。实验室坚持“开放、流动、联合、竞争”的运行方针，成为开展探索、创新和重大关键技术研究的基地和学术交流的平台，孕育培养了一批国防领域的高端科研人才。实验室主要研究方向：

· 电磁环境特性与电磁辐射危害防护研究

· 单舰及编队电磁兼容性预测与设计优化研究

· 电磁兼容性试验与测试研究

实验室通过条件建设项目，大幅度拓展提高了实验基础设施能力，建成了成体系且功能强大的电磁兼容试验设施群建设，基础设施能力处于国内领先、世界先进水平。实验室正在筹建的重大试验设施建设项目，建成后的各类电磁辐射源和测试设备等将极大地提升实验室在复杂电磁环境研究和试验方面的能力。

为把实验室建成国内一流的电磁兼容研究基地和学术中心，我们将努力建设一流的电磁兼容公共研究平台，聚集一流的 EMC 科研人才，创造一流的电磁兼容技术成果。围绕国防科技战略目标和武器装备技术的发展趋势，广泛开展高层学术交流，服务三军、服务国民经济建设，引领国内电磁兼容技术发展方向，推动国内电磁兼容技术不断地向前发展。

Shanghai Dongjun Information Technology Co., Ltd.

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Shanghai Dongjun Information Technology Co., Ltd. is the first Chinese high-tech enterprise, not only independently developing the commercialized full-wave electromagnetic software, but also providing teachnical services (e.g. Consulting, designing and solutions). With the breakthrough of numerical simulation methods for electrically large (or huge) systems and electromagnetic/photoelectric complex materials, Shanghai Dongjun has special advantages on the simulating electromagnetic large systems (antenna array, radome, RCS, EMC, metamaterial, microwave anechoic chamber, electromagnetic environment and mobile communication, etc.) and complex photoelectric system (laser, LED, photonic crystal and other optical communication devices and systema, etc.) The costumers of Dongjun cover the private/government research institutes, enterprises and universities in China and abroad.

As a domestic company in China, adhering to the “profession”, “integrity” , operating theory and taking “scientific innovation”, “custom-centered”, “brand development” as strategy, Dongjun is striving to become an international first-class electronmagnetic-wave/photoelectric software and service provider.

上海东峻信息科技有限公司是中国第一家自主开发商业化电磁波 / 光电仿真软件的企业，也是集产品研发、市场销售、技术服务为一体的高新企业。基于长期研发，上海东峻在电磁波（天线阵 / 天线罩、电磁隐身、电磁兼容 / 环境、微波暗室、电磁环境和移动通讯）和光电（激光、LED、超构材料、光子晶体、光通讯器件）等仿真技术方面取得突破性进展，尤其在大体系严格仿真计算和材料建模等方面形成独特优势。产品和服务的主要客户是科研所、企业、大学和国际用户。

作为一个本土企业和长期深耕中国电磁波 / 光电市场的研发型企业，公司秉承“专业、诚信”的经营理念，以“科技创新”、“客户为中心”、“品牌发展”为战略，力争成为国际一流的电磁波 / 光电仿真软件和服务提供商。

Unikinfo Technologies Co., Ltd

北京优诺信创科技有限公司

Unikinfo Technologies Co., Ltd is founded in 2007 which the headquarter is located in Beijing. The idea of our company is 'Independent research and development, Continuous innovation'. In the area of Complex EM environment simulator test, Radar/communication electronic information system simulation and test, RF & MW simulation and other related areas, we have a series of products which own the intellectual property rights and competitive products. The Unikinfo is a science and technology innovation enterprise with software and hardware.

Our businesses cover many military fields' areas such as aerospace, aviation, shipbuilding, electronics industry. We provide the service of advanced R&D design, products test and customized consulting to help customers improve R&D strength, shorter cycle round and reduce cost. We are aiming to build high level's equipment together with the customer. Unikinfo, Know The Single!

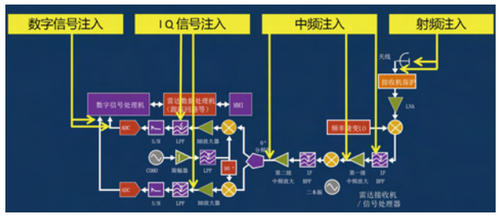
Introduce of products

Complex electromagnetic environment simulator

Complex electromagnetic environment simulator can build any complex EM environment. By building the electronic equipment mathematical model, radio wave propagation model and countermeasures model, it can simulate the process of the electromagnetic radiation, electromagnetic interference and electronic reconnaissance and attack. The simulator make various forms of electromagnetic signal. Produce the digital signal, intermediate frequency signal and Rf signal, build hardware-in-the-loop simulation system to meet the environment of the equipment under complicated electromagnetic environment adaptability, functions, performance verification and other test requirements.

· hardware-in-the-loop simulation

Base on the hardware, make the simulation of electromagnetic information generate at different stages of signal form. Like the RF microwave signal to get to the radar receiving antenna, medium frequency signal to get to the medium frequency processor, digital baseband signal to get to the signal processor to simulate and test the half physical closed loop of system.



· test in the outfield

· Build the simulator of outfield test

The natural environment, hydrology and meteorology, electromagnetic environment in the background

· Test plan formulation, inference and evaluation

· System of a complex electromagnetic environment signal generation

Movable type, fixed radar, communication, interference, target and clutter field simulation system.

· True value measuring and recording system

Broadband electromagnetic signal monitoring system; collection, storage and playback system

· Outfield test complex electromagnetic environment evaluation analysis system

High power microwave component simulation test system

Microwave test system

Microwave test system is used to evaluate the micro discharge suppression performance of the upper satellite power microwave component in the outer space environment. The detection method adopts the mainstream zero detection method and harmonic detection method. It has been developed more sets of micro discharge tests successfully for several military research institutes covering low frequency power of kilowatt, like L-band, S band, C band and K band. The high frequency can achieve several hundreds' watt level. Our company has the capability to build the multi-carrier microwave test system to support 10 lines microwave.

Passive intermodulation testing system

Passive intermodulation testing system is mainly used to evaluate whether passive intermodulation products meet the specifications' design produced by nonlinear factors such as antennas, feeders, filters and other high-power passive devices. The system can do 3, 5, 7, 9, 11, 13, 15 order PIM test with reflection /transmission mode, the output power can reach up to 200W per carrier. The Unikinfo has successfully developed several sets of passive intermodulation testing systems, which support up to four carriers testing, the 3rd order residual intermodulation is lower than -105dBm@2 * 50dB. The system in conventional intermodulation test function further derived synthetic signal envelope, the fine tuning of carrier phase control, real-time tiny signal receiving and other functions, providing a strong support for the research on further intermodulation products.

Digital multi-beam test system

Digital multi-beam antenna testing system is used together with horizontal near field testing system to do multi-beam antenna testing and verification working up to 40GHz. The system can receive signals from multi testing channels (64 channels typically) and one reference channel signal from antenna array. It can process the amplitude and phase of each signal with real time calculation to get the relative amplitude and phase result of each testing channel. Through the data post-processing, users can achieve the test of antenna array of any wave's directional image, axial ratio and direction.

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Rflight Communication Electronic Co., Ltd.

南京纳特通信电子有限公司

Founded in 2004, Rflight Communication Electronic Co., Ltd. is a high-new technology enterprise dedicated to R&D, manufacturing, sales, service and system solutions for RF power amplifiers, PIM testing systems and switch matrix. Product applications including defense, EMC, space research, high energy physics, wireless communications, calibration inspection, medical etc.

The company is headquartered in Jiangning High-New Technology Development Zone,with overseas offices in Germany, India, USA, domestic offices, R&D center, open-lab in Beijing, Shanghai, Xi'an, Chengdu, Shenzhen, Dongguan. We have a team of experienced microwave telecom R&D engineers amongst them over 20% are with senior engineer title. To cope with customer and market demand for the high quality power amplifiers and systems, our 130 person staff is determined to provide with creative solution that is on the cut-edge of domestic and international technology.

Our major products including various power amplifiers, PIM testing systems, Switch matrixes etc. Our Power Amplifiers freq. span from 4KHz-100GHz, power from 1Watt-500KWatt. R&D, manufacture capability: CNC, Anechoic chamber, Shield room, high-low temperature chamber, vibration table etc, the company is ISO9001 quality management system certified so that to ensure all the quality process have been controlled. In 2008, Rflight has signed agreement with Keysight Technolgy (formerly Agilent Technolgy) as official Solutions Partner to co-develop PIM and EMC testing platform.

Our products are FCC&CE certified for US & European markets. Our customers spreading over 10 countries all over the world, including China, USA, Germany, Sweden, India, Japan, Korea, Canada, France, Australia etc…

Company target: Domestically based company however with worldwide vision,to establish a leading company and create first class branding! Meeting defense and commercial customer requests as for Power Amplifiers and Application System Solutions.

To be the best and to be number one! is our vision, to generate value-add for customer is our guideline!

南京纳特通信电子有限公司成立于 2004 年，是一家专业从事射频功率放大器、无源互调测试系统、天线测试系统和开关矩阵研发、制造、销售、服务的高新技术企业。应用领域包括电磁兼容、空间探索、高能物理、无线通信、计量检测和医疗设备等。

公司坐落于南京市江宁技术开发区内，现有员工 130 余人，其中本科以上学历占 60% 以上。在德国、印度、美国设有海外办事处，在北京、上海、西安、成都和广东建有办事处、研发中心和开放实验室。公司拥有一批经验丰富、技术精湛的研发团队，具备不断创新的精神，立足国内行业前沿的同时更关注国际领先射频功放技术的发展动态，致力于用优秀的射频功放产品和系统满足顾客和市场的需求。

公司主要产品包括射频功率放大器、无源互调测试系统、功率容限测试系统、天线测试系统和开关矩阵等。功放频率范围：4kHz–100GHz，功率范围：1W–500KW。

公司拥有加工中心、屏蔽暗房、高低温设备、振动台等生产测试设备和环境实验室，并通过 ISO9001 质量管理标准体系认证，确保产品质量在各个环节都得到有效的控制和保障。2008 年，公司签约成为是德科技 (前安捷伦科技) 的方案解决和系统集成商，在南方基地建有“华为－纳特－是德”联合实验室，并与泰尔实验室共同研究各类通信的测试方法和相关标准的验证实施。

公司已通过 CE 和 FCC 认证并打开欧美等国际市场，客户分布在美国、德国、瑞典、印度、日本、韩国、加拿大、法国和澳大利亚等 10 多个国家和地区。

公司目标：立足国内，面向全球，做先进的公司，创一流的品牌！服务于民用应用领域，振兴民族射频功放产业！

公司秉承“精工精品、创新卓越”的理念，以“为客户创造价值”为工作准则，成为功率放大器及应用系统制造和解决方案供应商！

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